MULTI-GIGABIT CMOS ANALOG-TO-DIGITAL CONVERTER AND MIXED-SIGNAL DEMODULATOR FOR LOW-POWER MILLIMETER-WAVE COMMUNICATION SYSTEMS

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MULTI-GIGABIT CMOS ANALOG-TO-DIGITAL CONVERTER AND MIXED-SIGNAL DEMODULATOR FOR LOW-POWER MILLIMETER-WAVE COMMUNICATION SYSTEMS

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To dad, mom, and bro

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1P7M	1 poly and 7 metals
4G	fourth-generation
ADC	analog-to-digital converter
ADE	Analog Design Environment
AGC	automatic gain control
AM	amplitude modulation
ASIC	application-specific integrated circuit
ASK	amplitude-shift keying
AWGN	additive white Gaussian noise
BiCMOS	bipolar complementary metal-oxide semiconductor
BER	bit-error rate
BPSK	binary phase-shift keying
BW	bandwidth
C	capacitor
CBGA	ceramic ball grid array
CDMA	code division multiple access
CMFB	common-mode feedback
CML	current-mode logic
CMOS	complementary metal-oxide semiconductor
dB	decibel
dBc	decibel relative to a carrier level
dBi	decibel referenced to isotropic gain
dBm	decibel relative to one milliwatt
DAC	digital-to-analog converter
DB	database
DC	direct current
DFF	D flip-flop
DNL	differential nonlinearity
DRC	design rule check
DSB	double sideband
DSBSC	double-sideband suppressed-carrier
DSP	digital signal processor
EA	error amplifier
ECO	engineering change order
EIRP	equivalent isotropic radiated power
ENOB	effective number of bit
ERBW	effective resolution bandwidth
FCC	Federal Communications Commission
FDD	frequency division duplex
FFT	fast Fourier transform

FOM	figure of merit
FSPL	free-space path loss
GigE	gigabit Ethernet
GBW	gain bandwidth
GSM	global system for mobile communications
HDMI	high-definition multimedia interface
HDTV	high-definition television
I	in-phase
IF	intermediate frequency
IFFT	inverse fast Fourier transform
INL	integral nonlinearity
IP	internet protocol
IR	impulse response
KCL	Kirchhoff's current law
LEF	library exchange format
LNA	low-noise amplifier
LO	local oscillator
LOS	line-of-sight
LPF	low-pass filter
LSB	least significant bit
LTE	long-term evolution
LTCC	low-temperature cofired ceramic
mVpp	millivolt peak-to-peak
MB-OFDM	multiband orthogonal frequency-division multiplexing
MOSI	master output slave input
MSB	most significant bit
NF	noise figure
NLOS	non-line-of-sight
NMOS	n-type metal-oxide semiconductor
OFDM	orthogonal frequency-division multiplexing
OOK	on-off keying
OP-AMP	operational amplifier
P_{1dB}	1 dB gain compression point
P_{sat}	saturated power level
PA	power amplifier
PAR	peak-to-average ratio
PD	phase detector
PEX	parasitic extraction
PLL	phase-locked loop
PM	phase modulation
PMOS	p-type metal-oxide semiconductor
PSK	phase-shift keying
PVT	process-voltage-temperature
Q	quadrature-phase
QAM	quadrature amplitude modulation

QOS	quality of service
QPSK	quadrature phase-shift keying
QVCO	quadrature voltage-controlled oscillator
R	resistor
RST	reset
RF	radio frequency
RTL	register transfer level
RX	receiver
SAR	successive approximation register
SCLK	serial clock
SDC	Synopsys design constraints
SDF	standard delay format
SFDR	spurious free dynamic range
SiGe	silicon germanium
SNDR	signal-to-noise plus distortion ratio
SNR	signal-to-noise ratio
SOC	system-on-chip
SPEF	standard parasitic exchange format
SPI	serial peripheral interface
SS	slave select
STA	static timing analysis
T_{buf}	propagation delay due to buffer
T_{latch}	propagation delay due to latch
T_{su}	setup time
T/H	track-and-hold
TDE	time-domain equalizer
TF	transfer function
TX	transmitter
U-NII	unlicensed national information infrastructure
UWB	ultra-wideband
VCO	voltage-controlled oscillator
VGA	variable-gain amplifier
VLSI	very-large-scale integration
WiMAX	worldwide interoperability for microwave access
WLAN	wireless local area network
WPAN	wireless personal area network
XNOR	exclusive NOR
XOR	exclusive OR

SUMMARY

With rapid advancements in semiconductor technologies, mobile communication devices have become more versatile and inexpensive over the last few decades. However, plagued by the limited lifetime of batteries, low power consumption has become an extremely important specification in developing radio electronic devices. The ever-expanding demand of consumers to access and share information ubiquitously at faster speeds requires higher throughputs and increased signal-processing functionalities at lower power and lower costs. With the availability of wideband spectra, the millimeter-wave frequency bands, such as 60 GHz and beyond, provide an opportunity to bring portable multi-gigabit WPAN and WLAN applications into reality.

This dissertation presents the first time a fully-integrated, broadband, sub-watt demodulator using mixed-signal design techniques for multi-gigabit receiver systems. The broadband demodulator features a 13 GHz quadrature down-converter and high-speed A/D converters at a total power budget of 60 mW. The quadrature VCO is measured separately to ensure proper oscillating frequency. Parallelly, an ultra-low-power, 3 mW, 3 GS/s, 3-bit flash A/D converter is implemented, optimized, and analyzed to satisfy the stringent power budget. Using a standard 1 V supply, the fully-integrated multi-gigabit quadrature demodulator in 90 nm CMOS technology requires neither external synchronization controls nor processing to demodulate a BPSK modulated signal up to 2.5 Gbps while maintaining an error-free transmission. With a maximum carrier synchronization range of 51 MHz, its minimum sensitivity is measured to be -39 dBm.

Using the same system, high-definition video streaming is also demonstrated at a nominal data rate of 1.485 Gbps.

Following the development of 13 GHz quadrature demodulator, an extremely high-performance, dual-mode, multi-gigabit demodulator is proposed, implemented, and integrated with the 60 GHz CMOS receiver front-end in 90 nm CMOS technology. High performance is achieved by incorporating a very-high-speed, 6.912 GS/s, 19 mW, 3-bit flash A/D converter, and a two-channel, time-interleaving digital signal processor throughout digital back-end. The next-generation quadrature demodulator achieves an error-free transmission up to 3.5 Gbps and consumes less than 100 mW from a standard 1 V supply. This demodulator supports both ASK and BPSK modulated signals with an improved minimum receiver sensitivity of -54.5 dBm.

The presented work provides a promising and practical solution to transfer a large multi-media digital content at an extremely low-power budget without performance penalty. The developed demodulator system, utilized both RF and mixed-signal design techniques, makes this research work compelling for many short-distance wireless applications as well as high-data-rate point-to-point links for fixed stations.

CHAPTER 1

INTRODUCTION

1.1 Motivation

Wireless technology has been predominantly promoted in the mainstream market since the Second World War. Increased consumer demands and technological improvements have made radio-based electronic devices essential in our society. With an ever-increasing demand for bandwidth, improvements to analog-to-digital converters (ADC) and mixed-signal demodulators are essential to accommodate the needs of consumers.

A wireless local area network (WLAN) operates ubiquitously in the license-free bands between 2.4 and 5.8 GHz [1]. WLAN systems are scalable and can be configured in various topologies to meet the needs of specific applications, replacing the need for wired connections. For example, mobile WLAN users can access real-time information at high-speed data rates of up to several megabits per second downlink. Bluetooth technology in the 2.4 GHz range also enables data connections between electronic devices, such as laptop computers, and cellular phones. The ZigBee specification provides a reliable and inexpensive solution for small devices, such as wireless headphones, offering low data rates and low power consumption. Despite these benefits, WLANs are not adequate for next-generation multi-gigabit wireless communication devices due to their confined bandwidth.

In 2001, the Federal Communications Commission (FCC) allocated an unprecedented 7 GHz bandwidth between 57 GHz to 64 GHz in the United States for unlicensed operation [2]. For the first time, sufficient spectrum has made possible multi-gigabit radio frequency (RF) links compared to the WLAN counterpart. There are many high data rate applications one can envision, such as wireless personal area networks (WPAN), wireless high-definition multimedia interfaces (HDMI), and point-to-point 60 GHz links. Moreover, high bandwidth availability allows the use of spectrally inefficient modulation schemes that are more tolerant of the limited performance in complementary metal-oxide semiconductor (CMOS) technologies. For example, amplitude modulation (AM) schemes can be realized using a circuit consisting of very few low-power components. Also, the phase-shift keying (PSK) modulation with low-order constellations is more robust to phase noise and receiver noise than the spectrally efficient modulation techniques typically used for traditional WLAN systems. Finally, the implementation of a multi-gigabit demodulator employing mixed-signal design techniques becomes attractive for the emerging opportunities, requiring high-speed ADC with low resolution (3-4 bits).

Developing high-speed ADC and broadband demodulator for wireless systems also offers many advantages over traditional analog demodulators. In today's technology, high-speed signal processing and data converters are incorporated in almost all modern multi-gigabit communications systems. They are key enabling technologies for scalable digital design and implementation of baseband signal processors. Ultimately, the merits of a high-performance mixed-signal receiver, such as data rate, sensitivity, signal

dynamic range, bit-error rate (BER), and power consumption, are directly related to the quality of the embedded ADCs.

The objective of this research is to focus on the analysis and design of high-speed ADCs and a novel broadband mixed-signal demodulator with a fully-integrated digital signal processor (DSP) composed of low-cost CMOS circuitries. The system is integrated in the next-generation millimeter-wave 60 GHz 90 nm CMOS receiver, and presents an innovative dual-mode solution to demodulate multi-gigabit binary phase-shift keying (BPSK) and amplitude-shift keying (ASK) modulated signals. This approach reduces the resolution requirements of the high-speed ADC, which dramatically reducing the power consumption for any multi-gigabit communications system without performance degradation.

1.2 Challenges

Any communications channel, such as a fiber-optic cable, or a radio band, can be characterized by three factors: bandwidth, noise, and average output power. Bandwidth refers to the range of optical, or electromagnetic frequencies that can be used to transmit a signal; noise is anything that can disturb the signal; average output power is equivalent to the average transmitted, or received signal power in a given wireless channel. The maximum amount of information that can be reliably transmitted over a communications channel is known as channel capacity and is governed by

$$C = W \cdot \log_2(1 + SNR), \tag{1.1}$$

where C is the information capacity of the channel in bits per second, W is the available channel bandwidth in hertz, and SNR is the signal-to-noise ratio in dB [3]. Often the SNR is expressed as

$$SNR = \frac{P}{N_0 \cdot W}, \tag{1.2}$$

where P is the received signal power in watts, and N_0 is the one-sided noise density in watts per hertz. As suggested by (1.1), the maximum possible data rate is proportional to channel bandwidth linearly and SNR logarithmically. However, there exists a saturated information capacity considering an unlimited bandwidth. This phenomenon can be shown and derived below using L'Hôspital' rule:

$$\lim_{W\to\infty} C = \lim_{W\to\infty}(W \cdot \log_2(1+\frac{P}{N_0 W}))$$

$$= \lim_{X\to 0} \frac{(\partial / \partial X)\log_2(1 + X \cdot P / N_0)}{(\partial / \partial X)X}$$

$$= \lim_{X\to 0} \frac{P / N_0}{\ln(2) \cdot (1 + X \cdot P / N_0)}$$

$$= \frac{P}{\ln(2) N_0}. \tag{1.3}$$

The saturated information capacity from (1.3) indicates that choosing an infinite channel bandwidth does not necessarily yield maximum data rate. In reality, the continuous bandwidth of any wireless communications channel is always band-

limited and stipulated by the FCC [4]. Therefore, considering a band-limited channel, millimeter-wave frequency band, such as 60 GHz or beyond, is able to provide a higher data rate compared to traditional wireless standards.

The coverage, throughput, and applications of any wireless standard are related to the available channel bandwidth. Table 1.1 summarizes the popular wireless standards that are used pervasively. Global system for mobile communications (GSM) and code division multiple access (CDMA) provide suitable networks for voice and data services, such as text messaging, up to hundreds of kilobits per second over a few thousand meters [5]. On the contrary, popular WLAN standards satisfy the requirements of relatively smaller coverage (less than hundred meters away from the access point), and at the same time offer higher speed (up to hundred megabits per second) applications, such as hot-spots, private and public wireless networking.

ZigBee and Bluetooth are broadly categorized as WPAN. However, ZigBee is classified as a low-rate WPAN for control and automation, while Bluetooth is focused on connectivity between laptops as well as more general cable replacement between small electronics. Compared to Bluetooth, ZigBee uses significantly lower data rate and lower power consumption, and works with small packet devices. These wireless technologies are not only geared toward different applications but also are not capable to extend to other applications. For example, ZigBee is designed to use a couple of batteries inside a device for months to years, while Bluetooth must rely on fairly frequent battery recharging. Therefore, the ratio of the battery life time between Bluetooth and ZigBee is about one to hundred.

Table 1.1: Wireless standards comparison.

Standard	GSM/GPRS, CDMA	802.11 (WLAN)	802.15.4 (ZigBee)	802.15.1 (Bluetooth)	WiGig Alliance, Wireless HD
References	[5]	[6]	[7]	[8]	[9], [10]
Frequency (GHz)	0.85, 0.9, 1.8, 1.9	2.4, 5	0.868, 0.915, 2.4	2.4	60
Bandwidth (MHz)	25, 60, 75	83.5, 605	0.6, 26, 83.5	79	7000
Data rate (Mbps)	0.144 +	54 +	0.02 – 0.25	0.72 +	1485 – 7000
Range (m)	1000 +	1 – 100	1 – 100 +	1 – 10 +	1 – 10
Focus	Long range voice / data	Internet browsing, Network	Control, Monitoring, Automation	Cable replacement	Multi-gigabit data rate
Key Success Factors	Quality, Reach	Coverage, Flexibility	Power, Reliability, Cost	Cost, Convenience	Speed, Performance, HDMI cable replacement

The maximum achievable data speed of the aforementioned wireless standards is only hundreds of megabits per second. This is not sufficient for future commercial, industrial, and military applications, where a multi-gigabit transmission is desired. With the available wideband spectra in 60 GHz band (defined by WiGig Alliance and Wireless HD [9], [10]), a large amount of information can be reliably transmitted over a wireless channel compared to the traditional wireless standards. Realizing wireless high-definition multimedia interfaces at this frequency carrier then becomes a promising solution. Figure 1.1 shows the available market HDMI cables from uncompressed 720p to 1440p. Calculations have shown that in order to transfer digital files inside a 25 GB Blue-Ray disc and a 9.4 GB DVD disc in less than a minute, a

minimum data rate of 3.33 Gbps and 1.25 Gbps are required. Unprecedentedly, the license-exempt 60 GHz band offers the needed spectra in order to accommodate those multi-gigabit data rates.

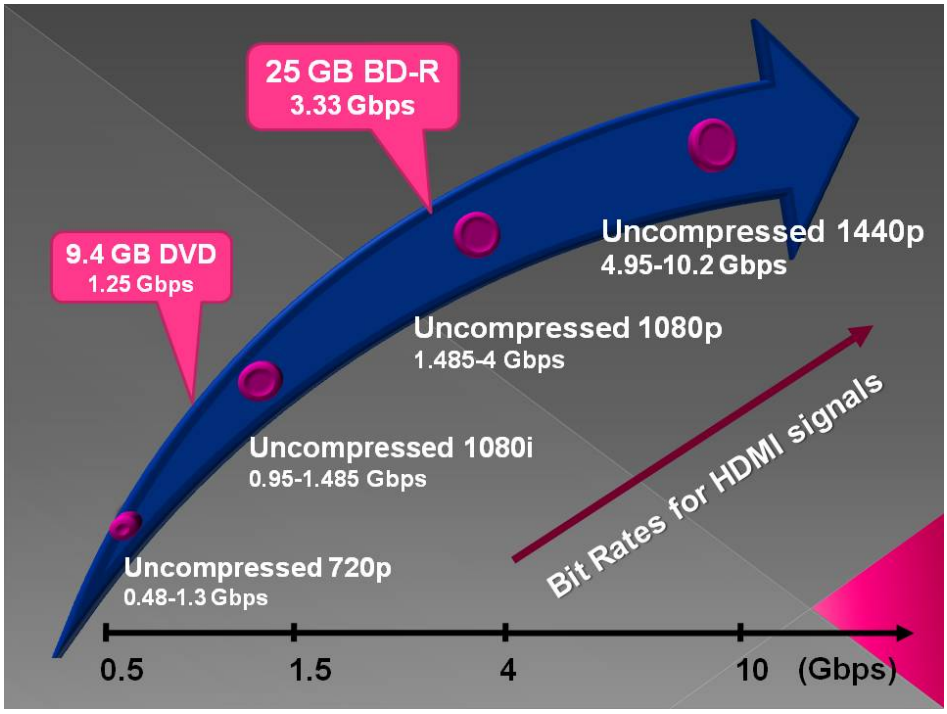

Figure 1.1: Market HDMI cable data rates.

Another approach to visualize the emerging market for HD television (HDTV) is to examine the required data rates for different HDTV standards. Unlike the multiband orthogonal frequency-division multiplexing (MB-OFDM) ultra-wideband (UWB) systems that can only support compressed video up to a data rate of 480 Mbps [11], the data rate for uncompressed video for HDTV interfaces can easily reach beyond 1 Gbps.

Depending on the progressive scan resolution and number of pixels per line, the required data rates vary from several hundred megabits per second to a few gigabits per seconds, as shown in Table 1.2. A typical HDTV resolution is 1920 x 1080 with a frame rate of 60 fps. Considering a RGB video format with 8 bits per channel per pixel, the required data rate is approximately 2.986 Gbps. In future, a higher number of bits per channel as well as higher refresh rates are expected to improve the quality of next-generation HDTVs. This can easily scale the data rate to well beyond 3 Gbps. Increased consumer demands and technological improvements certainly have imposed stringent specifications on the development of multi-gigabit integrated-circuit systems.

Table 1.2: Data rate requirements for HDTV standards.

Pixels per line	Lines per picture	Frame rate	Number of bits per pixel	Data rate (Gbps)
1280	720	24	24	0.531
1280	720	30	24	0.664
1280	720	60	24	1.327
1280	720	60	30	1.659
1920	1080	24	24	1.194
1920	1080	30	24	1.493
1920	1080	60	24	2.986
1920	1080	60	30	3.732

Driven by the available multi-gigabit audio/video interface for uncompressed data rates, increased on-chip processing speed is required. Scaling down the dimensions of transistors paves the roadmap for the next-generation transceivers systems. Since CMOS technology is by far the logic family with the highest circuit density, shrinking the

devices size is advantageous to those DSPs, baseband modem, and circuits that require/perform digital error corrections. Consequently, CMOS process becomes the chosen technology in this thesis work over its silicon germanium bipolar complementary metal-oxide semiconductor (SiGe BiCMOS) counterpart [12]. The enhanced performance of CMOS process comes from reduced parasitics due to metal interconnects with scaled devices. This inherently reduces the power consumption of individual circuit components using low supply voltage. However, as the technology is developed toward deep sub-micron regions (e.g., 90 nm), the matching characteristics of transistors become the dominant issue in designing high-speed ADCs [13], [96]. According to [14], a standard deviation of transistor random offset is approximately given by

$$\sigma_{VT} \approx \frac{A_{VT}}{\sqrt{W \times L}}, \tag{1.4}$$

where *Avt* is the transistor threshold mismatch coefficient, *W* is the width of a transistor, and *L* is the length of a transistor. Based on [13] and [96], a realistic trend of transistor threshold mismatch and voltage (V_{th}) at various CMOS technology nodes is compiled in Figure 1.2. Clearly, the threshold voltage does not scale linearly with the advanced CMOS technologies. This implies that as the supply voltage decreases, the usable dynamic range decreases, and the achievable signal-to-noise ratio (SNR) shrinks since the threshold voltage is already saturated at around 300 mV in 0.13 μm CMOS node.

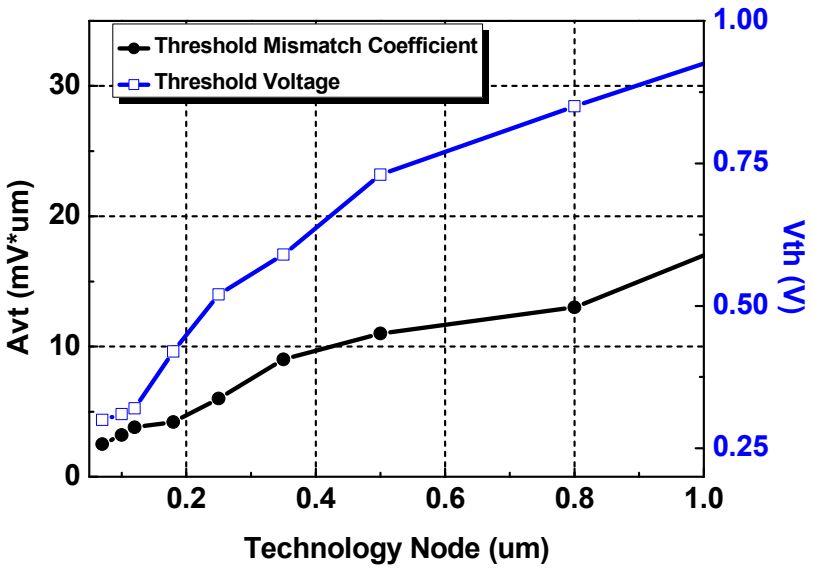

Figure 1.2: Transistor threshold mismatch and voltage at various technology nodes.

As technology advances to deep sub-micron nodes, the slope of the mismatch coefficient curve flattens out due to the increase in random mismatch. Subsequently, the linearity at the gigahertz sampling rate degrades. Table 1.3 compares the random offset between two technology nodes. The transistor aspect ratio, *W/L*, is chosen to be 4 for both cases. The threshold mismatch coefficient is then obtained from Figure 1.2. Substituting the parameters into (1.4), the input-referred static offset rms value for 1 μm and 90 nm nodes is calculated to be 10 mW and 16 mW, respectively. This indicates a high-speed penalty resulting from the mismatching characteristics in deep sub-micron CMOS technologies.

Lowering the total cost of each wireless node is vital to the success in volume applications. Hence, a fully-integrated CMOS solution is desired to avoid external

components. In contrast to the superior performance of digital circuits, the improved performance of analog circuits cannot be guaranteed by technological scaling. This requires special design techniques or calibration methods to guarantee yield and reliability. Therefore, operating at gigahertz sampling speed, the design of embedded ADCs and mixed-signal demodulator inevitably becomes a big challenge at the same time trying to satisfy the stringent power budget for mobile applications.

Table 1.3: Standard deviation of random offset between 1 µm and 90 nm nodes.

Technology Node	1 µm	90 nm
***Avt* (mV * µm)**	20	3.2
W / L	4	4
σ_{VT}	10 mV	16 mV

1.3 Organization of the Dissertation

This dissertation is divided into seven chapters. After discussing the research objective and challenges in Chapter 1, Chapter 2 begins with a review of available millimeter-wave communications channels, namely the 60 GHz and the 70-80-90 GHz bands. The performance trade-offs between wireless receivers architectures are analyzed, and an example of 60 GHz link budget analysis is given based on the state-of-the-art 60 GHz CMOS front-end specifications survey. The limitations due to CMOS millimeter-wave front-end are also incorporated into system-level simulation to justify suitable modulation schemes for multi-gigabit systems. Chapter 2 concludes with a comparison summary of various digital modulation schemes.

Chapter 3 introduces the practical high-speed ADC architectures with associated fundamental limits to performance in high-data-rate systems. The effects of quantization noise, thermal noise, aperture jitter, and resistor bowing are discussed thoroughly. Aperture jitter is identified as one key bottleneck for gigahertz sampling applications, requiring a very-precise clock source. In addition, a review of state-of-the-art ADCs in CMOS technologies is analyzed and compared. Those state-of-the-art ADCs are evaluated based on energy efficiency versus sampling frequency.

Chapter 4 explains the standard-cell based application-specific integrated circuit (ASIC) design flow. The ASIC design flow comprises of two stages. The first stage discusses digital front-end design, which takes a high-level Verilog description and synthesizes it into an optimized gate-level netlist. Static timing analysis (STA) is performed and verified using standard-cell libraries. The digital back-end design emphasizes on the place-and-route procedure and physical timing constraints. This is an absolutely critical design stage, where high-speed digital integrated circuits are optimized for timing and interfaced with analog circuits.

A low-power coherent BPSK demodulator system in 90 nm CMOS technology, employing mixed-signal design techniques, is discussed in Chapter 5. By minimizing the input-referred noise of comparator and reducing the propagation time of digital cells, an ultra-low-power 3-bit flash ADC is demonstrated. Next, the theory of operation of the coherent BPSK demodulator is discussed, and parameters to optimize the system are shown. The circuit building blocks consist of a 13 GHz quadrature voltage-controlled oscillator (QVCO), two passive double-balanced Gilbert-cell mixers, baseband amplifiers

with automatic gain-control (AGC) loop and DC offset compensation loops, two high-speed ADCs, a baseband DSP, and a high-speed digital-to-analog converter (DAC). This system demonstrates, for the first time, a unique method to demodulate a BPSK modulated signals up to 2.5 Gbps.

A dual-mode mixed-signal demodulator integrated with 60 GHz RF front-end is presented in Chapter 6. A high-performance ADC design employing resistive averaging technique in combination with high-speed integrated circuits is discussed first. High performance is achieved by sampling the ADCs at 6.912 GS/s, which is twice the rate achieved in Chapter 5. Finally, using the same analog quadrature front-end, a dual-mode demodulator is implemented to support ASK/BPSK modulated signals. Details of measurement results are discussed.

The contributions of this research work are summarized in the final chapter. Potential future research opportunities are also discussed in the end.

CHAPTER 2

MILLIMETER-WAVE COMMUNICATION SYSTEMS

2.1 Introduction

This chapter visits the current technologies that are suitable for millimeter-wave communication systems. The advantages and disadvantages of each frequency standard are discussed. Based on the requirements for multi-gigabit wireless applications, the receiver architecture and digital modulation scheme are carefully selected to satisfy target specifications. In addition, the state-of-the-art millimeter-wave front-end in CMOS technology is evaluated and an example of 60 GHz link budget analysis is shown. This chapter builds up the framework to realize a portable, robust, low-cost, low-power, and high-speed demodulator system in 90 nm CMOS technology.

2.2 Current Technologies Overview

Three frequency spectrums, such as UWB, 60 GHz band, and 70-80-90 GHz bands, are good candidates for high throughput wireless systems. In February 2002, the FCC officially unleashed a continuous bandwidth from 3.6 GHz to 10.1 GHz in the United States for UWB technology [11]. The emitted power spectral density of UWB signal is further kept under -41.3 dBm/Hz for indoor use and handheld devices [15]. This ensures an interference-free channel for the co-existing narrowband technologies, such as

the traditional 802.11, unlicensed national information infrastructure (U-NII), and proprietary licensed radar. Nevertheless, the required information capacity to establish a multi-gigabit wireless link is circumscribed by the maximum radiated power and the channel bandwidth. Therefore, 60 GHz and 70-80-90 GHz bands become the main frequency spectrums of interest to realize multi-gigabit applications.

2.2.1 60 GHz Band

2.2.1.1 Short-Distance Wireless Applications

Radios operating in the license-free 60 GHz band have unprecedented opportunities compared to radios operating in the traditional 2.4 GHz and 5 GHz license-free bands. The 60 GHz band features a large amount of bandwidth and a large worldwide overlap. This implies that a very high volume of data information can be transmitted wirelessly, enabling multi-gigabit transmission. As shown in Figure 2.1, multiple applications benefit from this: wireless HDTV, mobile handheld devices, wireless laptop docking stations, extremely fast downloading, instantaneous data transfers, and point-to-point 60 GHz links for telecommunications backhauls. The majority of 60 GHz applications are going to be exploited for emerging personal computers and consumer electronics in an in-door, home, or office environment. This indicates that 60 GHz is a promising candidate band for wireless entertainment applications. For example, the 60 GHz radio can be adapted to a movie cabin, where 25 seats are playing movies simultaneously. If each seat has its own HDTV and is connected

to an access point in the cabin ceiling, each connection provides individuals a high-speed data stream at a very-good quality. Nevertheless, a successful implementation of such systems requires a mature 60 GHz radio technology, which is the focus in the remaining chapters.

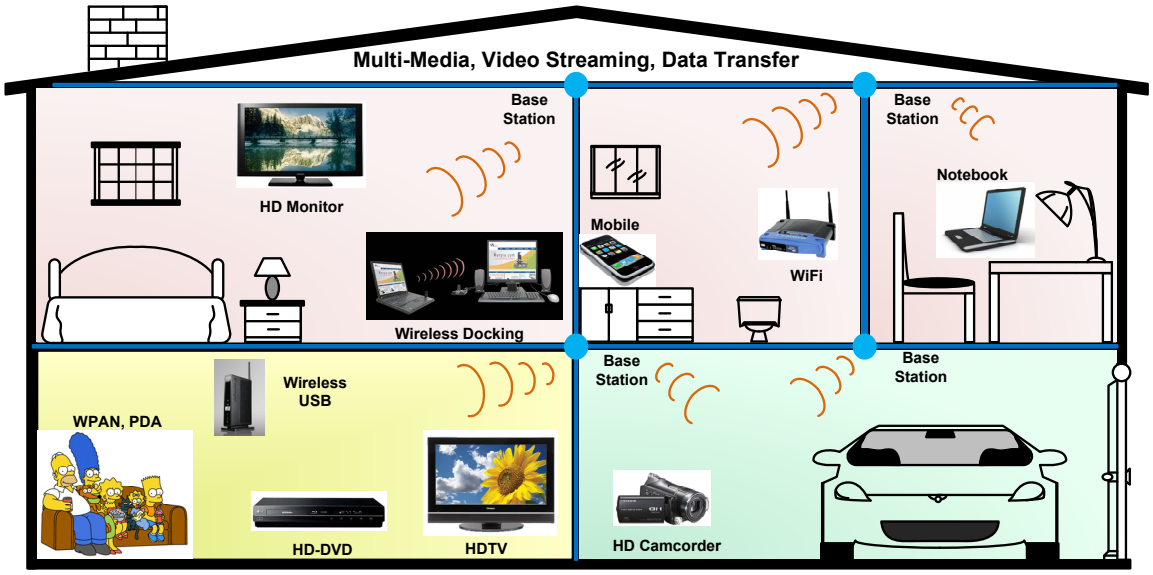

Figure 2.1: Examples of millimeter-wave multi-gigabit indoor applications.

2.2.1.2 Channel Characteristics

The license-exempt 60 GHz band provides tremendous research and market opportunities for next-generation wireless systems. Figure 2.2 shows the worldwide 60 GHz frequency allocations. The United States has been assigned the 57-64 GHz frequency band for general unlicensed usage. In Europe, the 62-63 GHz and 65-66 GHz bands have been provisionally allocated for mobile broadband systems, and the 59-62

GHz band is allocated for WLANs. This compares to < 700 MHz for all possible 802.11 or 802.15 channels. The plots of sea level and rain attenuations versus frequencies also reveal a unique property of 60 GHz. Unlike the 71-76 and 81-86 GHz bands, the 60 GHz millimeter-wave region of the electromagnetic spectrum is characterized by high levels of atmospheric RF energy absorption. This oxygen absorption weakens the 60 GHz signals over long distances.

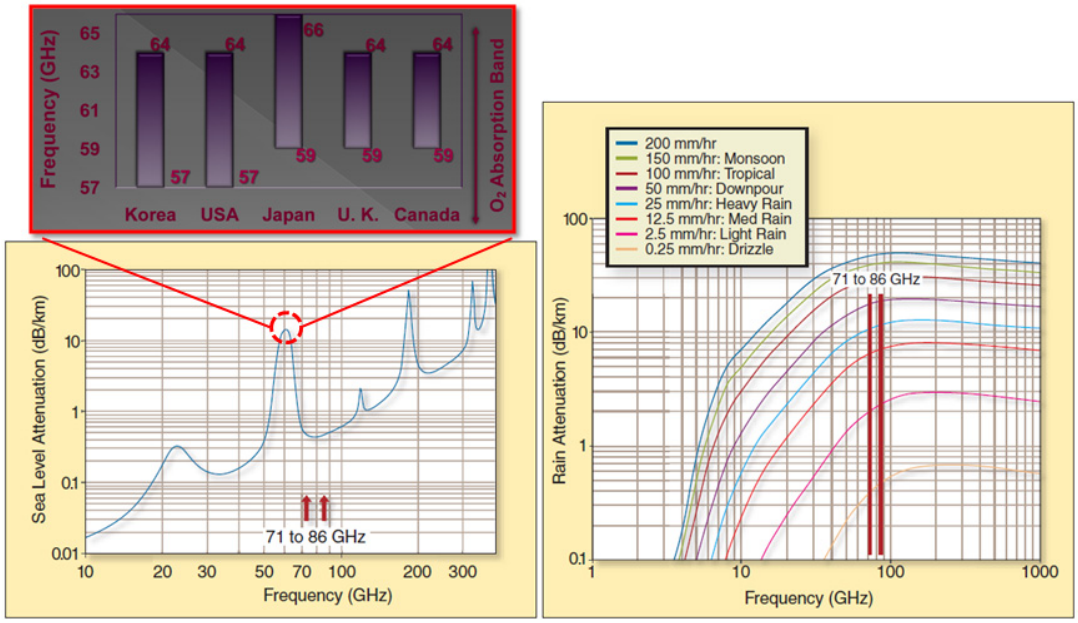

Figure 2.2: Sea level attenuation and rain attenuation [16].

Another benefit of the millimeter-wave frequency is the fundamental relationship between signal wavelength and antenna size. As RF frequency increases, signal wavelength becomes shorter, making it possible for smaller antennas to achieve the

required gain. To overcome the effects of atmospheric absorption, radio links in the millimeter-wave region must use narrow-beam width or high-gain antennas in order to focus as much of the transmitted signal as possible onto the receiving antenna [17]. This phenomenon offers interference and security advantages when compared to the traditional wireless standards. Figure 2.3(a) displays the emissions to the surrounding air space from an omnidirectional antenna that radiates in all directions and wastes the majority of the energy. On the other hand, Figure 2.3(b) depicts emissions from a directional antenna that radiates more effectively in one direction to provide higher gain by using narrow-beam antenna. This approach reduces the probability of receiving interferences and the amount of energy wasted in transmitting.

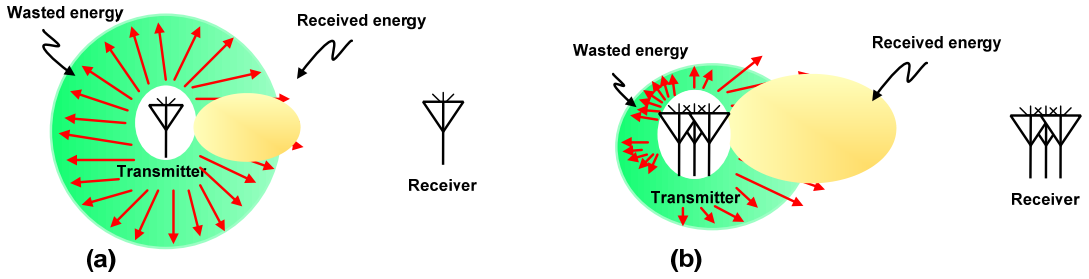

Figure 2.3: Space occupied by emissions from (a) an omnidirectional transmitter antenna and (b) a directional transmitter antenna.

The use of a directional antenna also improves the overall sensitivity of a radio link. The directivity of an antenna, when properly aligned (refer to Figure 2.3(b)), gives additional gain to the signal over wireless link [18]. Therefore, a very-compact low-cost

antenna can be implemented at 60 GHz to achieve a highly-focused beam. Comparing to 2.4 GHz or 5 GHz system, the form factor of millimeter-wave systems is considerably smaller and can be conveniently integrated into consumer electronic products.

2.2.1.3 Channel Considerations

Partly due to the unique 60 GHz characteristics, the FCC allows much higher transmitted power compared to other existing WLANs and WPANs systems to overcome high path loss and energy absorption at 60 GHz. This confines the 60 GHz operation to within a room or indoor environment [19]. In the United States, the FCC rules allow emission with an average and maximum power density of 9 $\mu W/cm^2$ and 18 $\mu W/cm^2$, respectively, at three meters from the radiating source [20], which is equivalent to an average and maximum equivalent isotropic radiated power (EIRP) of 40 dBm and 43 dBm, respectively. The FCC also specifies that the total maximum transmitted power of 500 mW for an emission bandwidth greater than 100 MHz. In mobile applications, 500 mW is considerably high power. From (1.1), a large channel bandwidth coupled with a high allowable transmitted power implies a higher possible information capacity. In other words, a high transmitted power in combination with narrow-beam high-gain antennas compromises the Friis's free-space propagation model with line-of-sight (LOS) path [21]. The received signal can be expressed in linear and logarithmic forms as follows:

$$p_r = \frac{p_t g_t g_r \lambda^2}{(4\pi)^2 d^2 l}, \tag{2.1}$$

where p_r is the received power in mW, p_t is the transmitted power in mW, g_t is the transmitter antenna gain in linear, g_r is the receiver antenna gain in linear, d is the distance from the source in meters, λ is the RF signal wavelength in meters, and l is the additional loss in linear, and

$$P_R = P_T + G_T + G_R - 20\log_{10}(\frac{4\pi \cdot d}{\lambda}) - L, \tag{2.2}$$

where P_R is the received power in dBm, P_T is the transmitted power in dBm, G_T is the transmitter antenna gain in dBi, G_R is the receiver antenna gain in dBi, and L is the additional loss in dB. The free-space path loss (FSPL) refers to the loss in signal strength of an electromagnetic wave over the air from a LOS path, and can be expressed as

$$FSPL = \left(\frac{4\pi \cdot d}{\lambda}\right)^2 = \left(\frac{4\pi \cdot d \cdot f}{c}\right)^2, \tag{2.3}$$

where c is the speed of light in free space in meters per second, and f is the carrier frequency in hertz. (2.1) and (2.2) suggest that the transmitted power has to be increased by a factor of four to double the coverage distance. In other words, given the same transmitted power, propagation attenuation due to (2.3) is directly proportional to the square of the radio frequency. In addition to Friis's propagation rule, the transmitted power using a low supply voltage limits a long-distance coverage at 60 GHz for wireless consumer applications.

2.2.2 70-80-90 GHz Band

2.2.2.1 Channel Characteristics

Frequencies between 30 GHz and 300 GHz, represented wavelengths from one to ten millimeters, are known as the millimeter-wave. On October 16, 2003, the FCC established service rules to promote non-Federal Government development through the use of 13 GHz millimeter-wave spectra in the 71-76 GHz, 81-86 GHz, and 92-95 GHz bands (also known as the E-band) in the United States [16], [23], [23]. These frequencies, as opposed to the 60 GHz frequency, do not suffer from oxygen absorption. Furthermore, the 92-95 GHz allocation is segmented into four unequal portions: 92-92.3 GHz and 93.2-94 GHz bands for unlicensed indoor devices, and 92.3-93.2 GHz and 94.1-95 GHz for licensed fixed, mobile, and radiolocation [24]. The 90 GHz band has also been investigated for imaging and remote sensing applications. This frequencies allocation forces lower data throughputs and creates more difficult filtering schemes.

2.2.2.2 Channel Considerations

The same usage of antennas, discussed in the previous section, also applies here. The shorter wavelength of the E-band permits the use of smaller antennas than would be required in the traditional WLAN frequencies to achieve higher directivity and higher gain. Unlike the 60 GHz band, high directivity coupled with high free-space loss without an electromagnetic attenuation due to oxygen absorption at these frequencies makes the E-band attractive for high-speed point-to-multipoint applications [25]. When smaller

high-directional antennas at millimeter-wave bands are placed in a given area, the net result is higher reuse of the spectrum, deriving to a higher density of users over distances of miles.

2.2.2.3 Millimeter-Wave Applications

Nowadays, government and business are demanding high-bandwidth and low-latency communication connections to transmit broadband information using a millimeter-wave band with a wider frequencies allocation. In order to replace wire-line and fiber transmission based systems, the 71-76 GHz and 81-86 GHz bands could potentially be used as a replacement for fiber optics, point-to-point backhaul systems, and broadband internet access, as shown in Figure 2.4. Unlike the fiber based systems that can be inadvertently damaged at any point between buildings or areas of a city, radios can be installed in inaccessible locations, such as on the sides of buildings, and towers. The point-to-point gigabit Ethernet wireless (GigE Wireless) technology also offers lower cost and time-efficient installation, while carrying the fiber-equivalent capacity over distances of a few miles [26]. For example, by exploiting E-band (refer to Figure 2.4), one can envision many applications, such as enterprise internet protocol (IP) networks, real-time HD perimeter security monitoring, and large data transfers.

Furthermore, wireless backhaul solutions using E-band are attractive for using multiple surveillance cameras ubiquitous in locations, such as government buildings. These cameras generate hundreds of digital video feeds to real-time monitoring stations.

The deployment of robust high-throughput backhaul systems offers a compelling, low-latency, high-quality video solution to time-sensitive, bandwidth-hungry digital video feeds. The 70-80 GHz band creates a more secure and less vulnerable network compared to the wired networks.

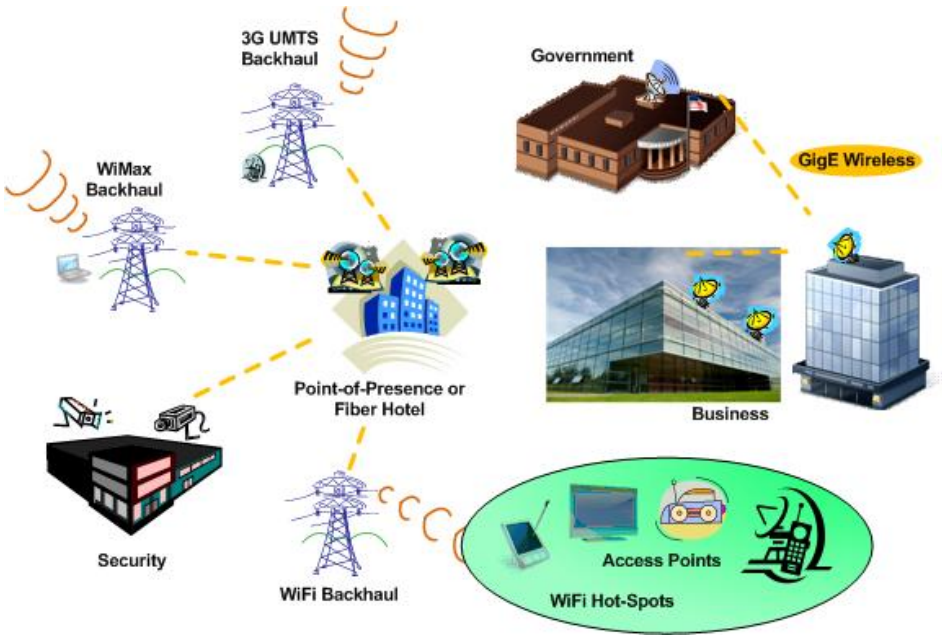

Figure 2.4: Examples of millimeter-wave applications over distances.

2.2.3 Summary

Figure 2.5 summaries and compares all the important wireless technologies available up to date. These technologies are compared based on data rate versus distance coverage.

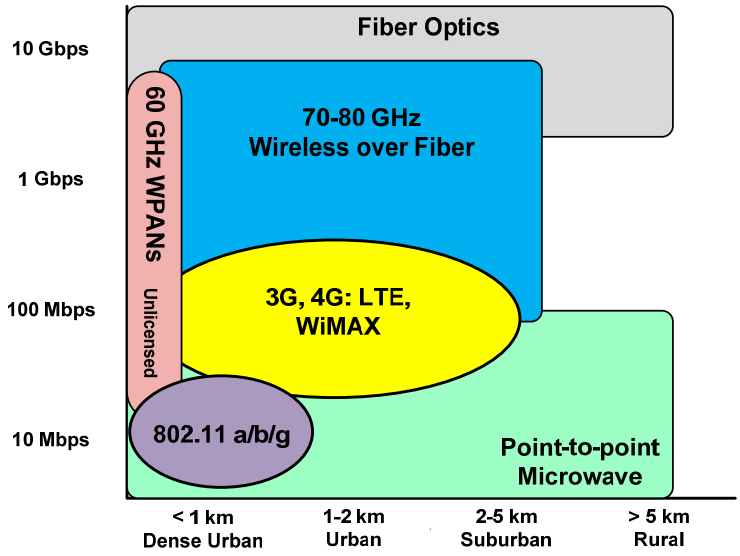

Figure 2.5: High-capacity wireless landscape.

The Wi-Fi solution (802.11a/b/g) is a license-free short-distance multi-access technology that is popular for local area residential or hotspot connectivity. Like most technologies, Wi-Fi has a number of limitations that makes it impractical for high-capacity transmission. On the other hand, the fourth-generation (4G) wireless systems, such as worldwide interoperability for microwave access (WiMAX), and long-term evolution (LTE) technologies, offer a substantial increase in throughput and address many of the quality of service (QoS) issues inherent with Wi-Fi. However, theoretical data rates of tens of megabits per second are possible. Furthermore, fixed wireless radios operating in the microwave band from 6 GHz to 38 GHz are widely used for connecting together cell sites and providing point-to-point data connectivity. For example, the microwave backhaul solution is suitable for fixed wireless transmission over a distance of a few kilometers, but these microwave bands are limited by the relatively narrow

channels up to 28 MHz [27]. The high-capacity wireless system, such as the E-band, provides the largest system capacity operating at multi-gigabit data rates over the air. However, the E-band charges license fee, and consumes high power in the base station. Considering power consumption, data rate, and antenna size, the license-exempt 60 GHz band is still the most compelling solution for short-distance multi-media applications, and captures worldwide availability.

2.3 Wireless Receivers

The receiver architecture in a wireless system is extremely important in determining power dissipation, cost, and complexity [28]. Strong interferers in the frequency channel can be removed using channel selection filters, whose quality factor, in-band loss, and out-of-band rejection ratio depend on the chosen topology and process. Band-pass filters are usually implemented in the receiver to attenuate the unwanted local oscillator (LO) leakages and image frequencies.

2.3.1 Homodyne Receivers

In telecommunication, a homodyne receiver is also known as direct-conversion, synchrodyne, or zero-IF receiver [29]. This architecture directly translates the RF signal to baseband in a single frequency-translation step by matching the LO frequency and RF carrier frequency. The block diagram of a homodyne receiver is shown in Figure 2.6.

Homodyne architecture is the most simple receiver architecture compared to the heterodyne receivers and low-IF receivers. This implies that the overall receiver system employing direct-conversion architecture dissipates least power and is suitable for monolithic integration.

However, using fewer components in the homodyne receiver does not guarantee sufficient sensitivity. For example, prior to the single direct-conversion step, the RF signal is usually gain-limited at high frequencies in CMOS technologies. As a result, after the down-conversion, a chain of amplifiers is implemented to meet the required sensitivity. The drawbacks are DC offset and flicker noise due to the increased complexity of baseband circuits. DC offset is created in the down-conversion mixer due to transistor random mismatch, poor isolation resulting LO leakage, and self-mixing term. Flicker noise is associated with the nature of CMOS device, and dominates the noise spectrum at low frequency (e.g., less than 10 MHz) [30].

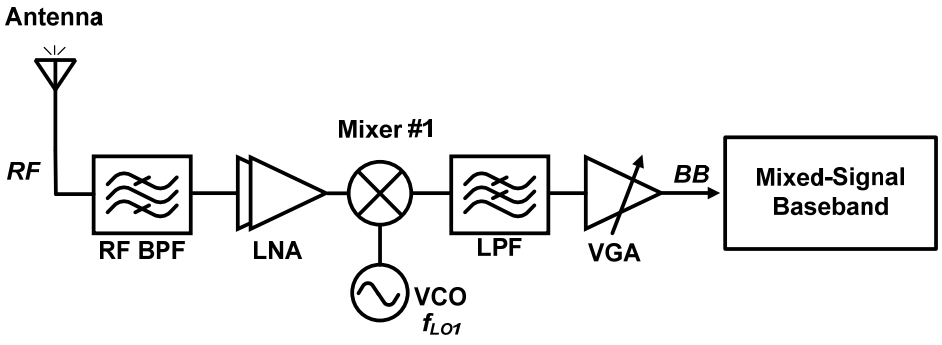

Figure 2.6: Homodyne receiver block diagram.

The complexity of modulation schemes is also limited in the homodyne architecture. Any modulation scheme that requires quadrature mixing and quadrature LO generation imposes circuit design challenges and reliability issues in CMOS technologies. For example, in a millimeter-wave homodyne receiver based on quadrature phase-shift keying (QPSK) modulation scheme, the LO source generates two single tones at 60 GHz. A reliable quadrature LO source is extremely difficult to realize at this frequency when I/Q amplitude imbalance and phase mismatch degrade SNR and BER. Therefore, alternative receiver architecture is investigated in the next subsection.

2.3.2 Heterodyne Receivers

Unlike the homodyne architecture, heterodyne architecture employs two down-conversion steps, followed by mixed-signal baseband circuits, as shown in Figure 2.7. The modulated RF signal is first down-converted to an intermediate frequency (IF). When the RF signal falls within millimeter-wave band, the input matching network of the low-noise amplifier (LNA) exhibits a band-pass response. Bandwidth should be chosen carefully to translate entire continuous RF bandwidth completely to IF without information loss. In addition, the IF signal is not expected to operate in millimeter-wave band because the low quality factor (< 10) of passive filters introduces substantial insertion loss due to highly conductive CMOS substrate in standard technologies [31]. After another down-conversion mixer (Mixer #2), the demodulation finally takes place. Clearly, the heterodyne architecture is more complicated, consumes more area and dissipates more power, compared to the homodyne architecture. Nevertheless, a

heterodyne receiver is much more robust in terms of receiver sensitivity, and supports higher-order modulation schemes. For example, a more accurate quadrature LO source can be realized on-chip at IF.

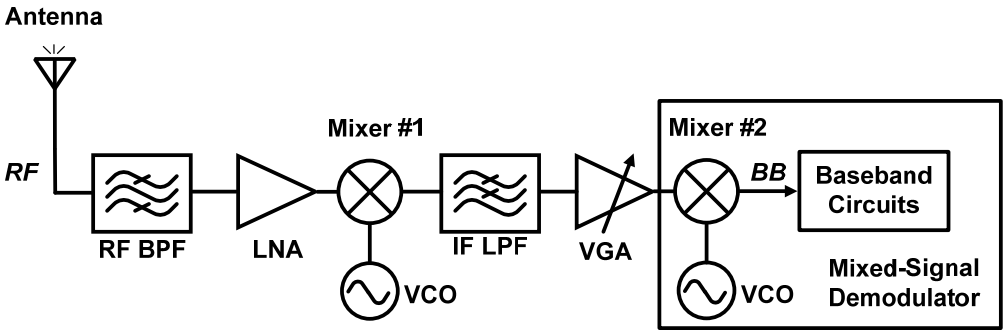

Figure 2.7: Heterodyne receiver block diagram.

The dominant issue in a heterodyne receiver is the image frequency due to mixing. The image frequency is undesired in receivers that can interfere with the desired RF signal [29]. As shown in Figure 2.8, the image frequency has equal spectral distance from the LO signal to the RF on the opposite site. Down-conversion through a mixer generates a sum as well as a difference term at the output. That is the frequency bands above and below the LO signal are both down-converted to the same IF. If the desired signal is f_{RF}, where $f_{RF}=f_{LO1}+f_{IF}$, then the signal at the frequency $f_{IMAGE}=f_{LO1}-f_{IF}$ is also down-converted to the same IF. The signal in f_{IMAGE} is the unwanted image signal. This image cannot be filtered out once it is down-converted to IF, and will directly impact the performance of the demodulator.

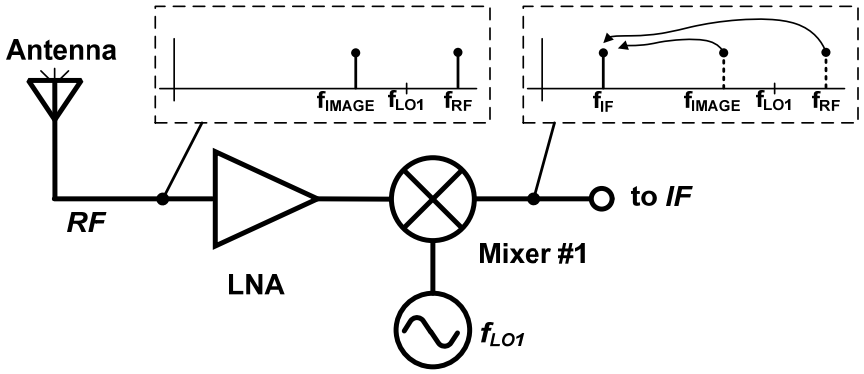

Figure 2.8: Image frequency in a heterodyne receiver.

Table 2.1: Trade-offs between homodyne and heterodyne architectures.

	Homodyne	Heterodyne
Advantages	1. Simplicity 2. Compact integrated circuits 3. Reduction of power consumption 4. Reduction of cost	1. Relaxed RF front-end designs 2. Medium-gain LNA 3. Better sensitivity and robustness 4. Higher data throughput
Disadvantages	1. Low-frequency flicker noise 2. Phase and amplitude imbalance 3. DC offset and leakage 4. Susceptible to intermodulations	1. Image rejection mechanism 2. Higher system-level integration

Table 2.1 summaries the advantages and disadvantages of homodyne and heterodyne architectures. In heterodyne, the advantages outweigh the disadvantages. Higher system-level integration will not increase the receiver area drastically as the CMOS technology advances to deep sub-micron regions. The required image rejection filter can be relaxed if the IF frequency is sufficiently far away from the LO signal. This can be achieved by choosing IF high enough so that the band-pass response of the front-

end LNA sufficiently rejects the image frequency after the antenna. However, circuit designs, such as amplifiers, filter, and mixer at the IF level will become another challenge with the increase in IF.

2.3.3 State-of-the-Art 60 GHz CMOS Front-End

As seen in the previous sections, the 60 GHz band delivers the widest continuous spectral channel and features license-free operation at the same time. Choosing heterodyne architecture, the 60 GHz environment represents an opportunity to realize a multi-gigabit radio that is not limited by modulation schemes. Then, the performance of a wireless transceiver is determined by the intrinsic and extrinsic noise sources. Typically, the extrinsic noise sources include transmitter (Tx) noise leakage in receiver (Rx) band, intermodulation distortion, quantization noise, and imperfectly filtered interference [32]. On the other hand, the intrinsic noise source is generated by the circuit element itself. Thermal noise and flicker noise are common intrinsic noise sources.

The coverage of a radio is limited by the transmitted power and governed by the Friis's free-space propagation model. In transmitter, the maximum output power of a power amplifier (PA) is determined by the supply voltage, circuit topology, and device modelling. On the other hand, the noise figure (NF) of a receiver is normally determined by the LNA following on-chip antenna. The performance of the LNA directly impacts the sensitivity of a receiver. To realize a low-cost single-chip 60 GHz transceiver, the state-of-the-art millimeter-wave front-end components are reviewed and summarized in Table

2.2. An integrated transmitter in 90 nm CMOS technology has reported to produce an output P_{1dB} of 4.1 dBm [35]. A small form-factor integrated antenna is also possible with low-temperature cofired ceramic (LTCC) materials in a thin cavity-down ceramic ball grid array (CBGA) package [36]. In receiver, a 90 nm CMOS millimeter-wave front-end, consisted of a LNA, a mixer, and a voltage-controlled oscillator (VCO), achieves a conversion gain of 24.8 dB and a double sideband (DSB) NF of 7.3 dB. These specifications can be used to analyze the coverage of 60 GHz radios.

Table 2.2: 60 GHz millimeter-wave front-end components.

Component	Year	Technology	Specification	Parameter	Unit	Ref.
PA	2010	65 nm CMOS	OP_{1dB} Psat	7.1 10.5	dBm dBm	[33]
PA	2010	90 nm CMOS	OP_{1dB} Psat	5.1 8.4	dBm dBm	[34]
Tx	2009	90 nm CMOS	OP_{1dB} Psat	4.1 8.6	dBm dBm	[35]
Antenna	2009	LTCC	Gain Beam width	11 30	dBi degrees	[36]
LNA	2009	130 nm CMOS	Gain NF	20.4 8.6	dB dB	[37]
LNA	2010	90 nm CMOS	Gain NF	15.7 6.2	dB dB	[38]
Rx	2010	90 nm CMOS	Gain NF	24.8 7.3	dB dB	[39]

2.3.4 Example of 60 GHz Link Budget Analysis

The sensitivity, dynamic range, gain, noise figure, and intermodulation products are the important specifications of wireless receivers. The receiver sensitivity refers to the

lowest RF input signal that must be detected and distinguished by the receiver. Usually, the noise performance of the receiver defines the sensitivity. The receiver thermal noise, caused by random movement of particles in the medium, is dependent on the signal bandwidth and temperature of the medium. For a properly working wireless link, the noise of the input signal is significantly higher than the thermal noise level. Using the above information, the receiver minimum sensitivity, P_{MIN}, can be expressed in logarithmic form as

$$P_{MIN} = 10\log_{10}(kT) + 10\log_{10}(BW) + NF + SNR_{MIN}, \tag{2.4}$$

where k is the Boltzmann constant, $1.38\text{x}10^{-23}$, in Joule/K, T is the absolute temperature in Kelvin, BW is the bandwidth occupied by the RF signal, NF is the noise figure of the receiver, and SNR_{MIN} is the minimum SNR required for the chosen modulation. SNR defines the energy per bit to noise power spectral density ratio (E_b/N_o) needed to compare the BER performance of different digital modulation schemes without taking channel bandwidth into account. To achieve a specific level of reliability in terms of BER, the baseband SNR required for a suitable modulation scheme can be calculated as

$$SNR_{ADC} = P_{IN} - 10\log_{10}(kT) - 10\log_{10}(BW) - NF, \tag{2.5}$$

where P_{IN} is the received input power level. A raw BER before error correction of 1E-06 is typically desirable for wireless communication systems [40]. For BPSK modulation, the theoretical SNR required for a BER of 1E-06 is 10.5 dB. Considering a zero link margin and using the integrated CMOS receiver front-end NF from Table 2.2, the receiver minimum sensitivity is computed to be -60.76 dBm, as shown in Table 2.3.

Table 2.3: Sensitivity analysis of a 60 GHz receiver.

Technology	Millimeter-wave 60 GHz	Unit
Carrier frequency	60	GHz
RF bandwidth	3.5	GHz
Modulation	BPSK	—
SNR @ 1E-06 BER	10.5	dB
Rx NF	7.3	dB
Calculated sensitivity	-60.76	dBm

The link budget is further analyzed using the system-level parameters based on the Friis's free-space propagation model with LOS path in (2.1) and (2.2). It can be evaluated based on two extreme distances: low-power mode and high-power mode. Low-power mode refers to short-distance coverage, whereas high-power mode represents the maximum deliverable distance. Using the information in Table 2.3, the minimum detectable input power, P_R, from (2.2) is -60.76 dBm. This case happens when the wireless link is at its maximum distance. As a result, the received power is at its minimum detectable level. Then, the Friis's free-space propagation model can be solved in terms of coverage:

$$d = \frac{\lambda}{4\pi} 10^{\frac{P_T + G_T + G_R - P_R - L}{20}}. \tag{2.6}$$

Table 2.4 summarizes the coverage performance. Approximately a wireless link of five meters can be achieved. This also justifies that the 60 GHz radio is suitable for short-distance multi-gigabit applications and next-generation WPANs. In case of non-line-of-sight (NLOS), a link distance of greater than ten meters can be easily achieved

with phased array systems [41]. However, the complexity and overall system power consumption are beyond the scope of this research work.

Table 2.4: Link budget analysis of a 60 GHz system.

Technology	Millimeter-wave 60 GHz		Unit
Transmitter power, P_T	4.1		dBm
Antenna gain, G_T	11		dBi
Antenna gain, G_R	11		dBi
Additional loss	5		dB
Received power, P_R	-60.76	-30	dBm
Calculated coverage	4.93	0.14	meter

2.4 Digital Modulation Schemes

In telecommunications, modulation is the process of conveying a message signal, such as a digital bit stream, inside a carrier signal that can be physically transmitted across the wireless medium. This section focuses on the trade-offs between various modulation schemes. Finally, the most suitable modulation schemes for 60 GHz wireless receivers are chosen based on CMOS millimeter-wave front-end limitations to performance, power, cost, portability, and robustness.

2.4.1 CMOS Front-End Performance Limitations

A more spectrally efficient modulation scheme, such as QPSK modulation, will produce twice the data rate compared to BPSK modulation. However, the demand to

increase data throughput in the same channel requires low phase-noise oscillator and low-distortion PA [42]. This limits the 60 GHz CMOS radio performance and modulation schemes.

Unlike the receiver noise figure that is primarily caused by random noise, the PA experiences nonlinear distortions. As the input power increases, the amplifier transfer function (TF) becomes nonlinear, and eventually its output saturates to a power level, P_{sat}. A qualitative measure of PA's linearity is to test its intermodulation distortion by applying more than one carrier frequency at its input [43]. The aforementioned distortion is an example of AM-AM distortions, where the input amplitude has a nonlinear effect on the output amplitude. In addition to AM-AM distortion, amplifiers also exhibit AM-PM distortions, where the output phase is nonlinearly affected by the input amplitude. This nonlinear phenomenon of amplifiers was described by Saleh [44]. Let the input signal to the PA be:

$$x(t) = r(t) \cdot \cos(\omega_0 t + \psi(t)), \tag{2.7}$$

where ω_o is the carrier frequency in radian, $r(t)$ is the modulated envelope, and $\psi(t)$ is the modulated phase. The corresponding output is written as

$$y(t) = A[r(t)] \cdot \cos(\omega_0 t + \psi(t) + \Phi[r(t)]), \tag{2.8}$$

where $A[r(t)]$ models the nonlinear gain error due to AM-AM conversion, and $\Phi[r(t)]$ represents the amplitude-dependent phase-shift error due to AM-PM conversion. The AM-AM and AM-PM effects are modeled:

$$A[r(t)] = \frac{\alpha_a \cdot r(t)}{1 + \beta_a \cdot r^2(t)}, \tag{2.9}$$

and

$$\Phi[r(t)] = \frac{\alpha_\Phi \cdot r^2(t)}{1 + \beta_\Phi \cdot r^2(t)}, \tag{2.10}$$

where α_a and β_a are the parameters to model the amplitude gain, and α_Φ and β_Φ are the parameters to compute the phase change for an input signal. In the following sections, system-level simulations are performed to observe degradations due to nonlinear PA and phase-noisy oscillator using the parameters from Table 2.5. For each constellation diagram, 1000 symbols are recorded. In addition to PA and LO noise sources, additive white Gaussian noise (AWGN) is also considered. This models the impairment to a channel by linearly adding white noise with a constant spectral density in watts per hertz of bandwidth. Wideband Gaussian noise comes from noise sources, such as thermal noise, shot noise, or black body radiations.

Table 2.5: Parameters for the non-ideal models.

Component	Specification	Parameter	Unit
PA	α_a	2.1587	—
	β_a	1.1517	—
	α_Φ	4.0033	—
	β_Φ	9.1040	—
	Transmitted power	4.1	dBm
LO	Phase noise	-95	dBc/Hz
	Carrier offset	1	MHz
AWGN	E_b/N_o	20	dB
	Data rate	2	Gbps

2.4.2 Amplitude-Shift Keying

Digital modulation techniques are classified into coherent and non-coherent techniques, depending on whether the receiver is equipped with a phase recovery circuit or not [3]. Non-coherent ASK is a commonly used modulation scheme in CMOS transceiver development because of its simplicity and low implementation costs [34], [38], [39]. On-off keying (OOK) is the special case of ASK modulation where no carrier is present during the transmission of a zero. A binary ASK signal can be defined by

$$s(t) = A \cdot m(t) \cdot \cos(2\pi f_c t), \qquad 0 \le t \le T_b \tag{2.11}$$

where A is a constant in volts, $m(t)$ is either logic one or zero, f_c is the carrier frequency, and T_b is the bit duration. When $m(t)$ is nonzero, its power is just the time average of energy given by

$$\lim_{T_b \to \infty} \frac{1}{T_b} \int_0^{T_b} |s(t)|^2 dt, \tag{2.12}$$

where $s(t)$ has an average power of $P = A^2/2$ and $A = \sqrt{2P}$. (2.11) can be expressed in terms of transmitted signal energy per bit:

$$s(t) = \sqrt{2P} \cdot \cos(2\pi f_c t) = \sqrt{PT_b} \cdot \sqrt{\frac{2}{T_b}} \cdot \cos(2\pi f_c t) = \sqrt{E_b} \cdot \sqrt{\frac{2}{T_b}} \cdot \cos(2\pi f_c t), \tag{2.13}$$

where $0 \le t \le T_b$, and $E_b = PT_b$ is the energy contained in one bit duration. If we take $\phi_1(t) = \sqrt{\frac{2}{T_b}} \cdot \cos(2\pi f_c t)$ as the orthonormal basis function of unit energy, the applicable

signal space or constellation diagram of the binary ASK can be depicted, as shown in Figure 2.9(a). The corresponding time domain response of the binary signal and OOK modulated signal is in Figure 2.9(b).

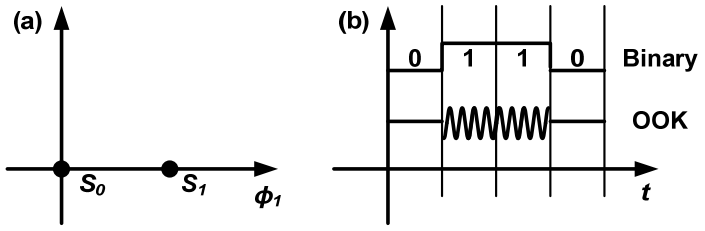

Figure 2.9: (a) ASK constellation diagram; (b) Binary and OOK modulated signals.

OOK modulation is known for its simplicity and low power consumption. During the transmission of a logic zero, the transmitter goes into idle mode. However, the penalty of using this scheme arises in the receiver side. In the presence of undesired signals, such as interference, multipath fading, LO leakage, and Rx leakage in a frequency division duplex (FDD) system, the sensitivity degrades significantly, and the OOK modulated signals become very vulnerable to these propagation effects.

2.4.3 Phase-Shift Keying

Unlike ASK modulations, PSK modulations employ coherent phase and frequency detection using analog, mixed-signal, or digital techniques. The PSK is widely

used in high-quality radio communications systems for a couple reasons. First, the output of PSK modulated signals is constant envelope and is not susceptible to interference compared to amplitude modulated signals. Furthermore, constant envelope leads to a more relaxing peak-to-average ratio (PAR). On the other hand, a common issue with PSK is that the receiver does not know the exact phase of transmitted signal to determine whether the binary signal corresponds to logic one or zero. Ways to overcome this problem are to incorporate phase-recovery circuits or to apply differential coding to the binary signal [45]. For example, a differential encoding is accomplished by making a change in phase equal to a logic one and no phase change equal to a zero. Using differential encoding, a non-coherent technique is another method.

In a coherent BPSK system, the pair of signals $s_0(t)$ and $s_1(t)$ used to represent binary symbols one and zero, respectively, is defined by

$$s_i(t) = \sqrt{\frac{2E_b}{T_b}} \cdot \cos(2\pi f_c t + \pi \cdot i), \qquad 0 \le t \le T_b \tag{2.14}$$

where E_b is the transmitted signal energy per bit, $i = 0$ for logic zero, and $i = 1$ for logic one. A constant envelope is maintained by alternating carrier phase by 180 degrees. QPSK modulated signals can be derived in similar fashion by dividing the carrier phase into four-equally-spaced orthonormal bases, such as π/4, 3π/4, 5π/4, and 7π/4:

$$s_i(t) = \sqrt{\frac{2E_b}{T_b}} \cdot \cos(2\pi f_c t + \frac{\pi}{4}(2i+1)), \qquad 0 \le t \le T_b \tag{2.15}$$

where E_b is the transmitted signal energy per bit, and $i = 0$ for logic zero in in-phase channel, $i = 1$ for logic zero in quadrature channel, $i = 2$ for logic one in in-phase channel, and $i = 3$ for logic one in quadrature channel. A two-dimensional signal constellation is required to map to these four message points. With four phases, QPSK can encode two bits per symbol, which is twice the rate of BPSK. In other words, the required bandwidth for QPSK is half of BPSK. Before the baseband filters are considered, to achieve a BER of 1E-08, the required SNR for BPSK and QPSK at the slicer is 12 dB and 12.15 dB, respectively.

After incorporating the effects of nonideal PA and phase-noisy LO, the simulated constellation diagrams of BPSK and QPSK are shown in Figure 2.10(a) and Figure 2.10(b), respectively. Several key points can be observed in the constellation diagrams. Although the constellation points are distorted, a SNR of 20 dB used in the simulation is sufficient to achieve error-free demodulation. Moreover, the rotational symbol jitter from LO phase noise and AM-PM nonlinearities is evident. This rotates and spreads the symbols from theoretical points. There is also a rotational tilt in counter clockwise direction, indicating a positive phase shift to the output signal. Because the PA is operating at its gain compression point, the additional phase is introduced by the AM-PM distortion. In addition to gain compression, the AM-AM conversion of PA results in a smaller average amplitude compared to ideal points. Lastly, since the model incorporates the effects of AWGN channel, and the SNR at the slicer is chosen to be 20 dB, the output symbols experiences an omnidirectional variation in amplitude. Figure 2.11(a) further simulates these nonidealities in a 16 PSK modulation system. The result shows that the

signal space of 16 PSK is extremely corrupted. This indicates that for high-order modulation schemes, SNR and LO performances are the most critical specifications for high-order PSK modulation.

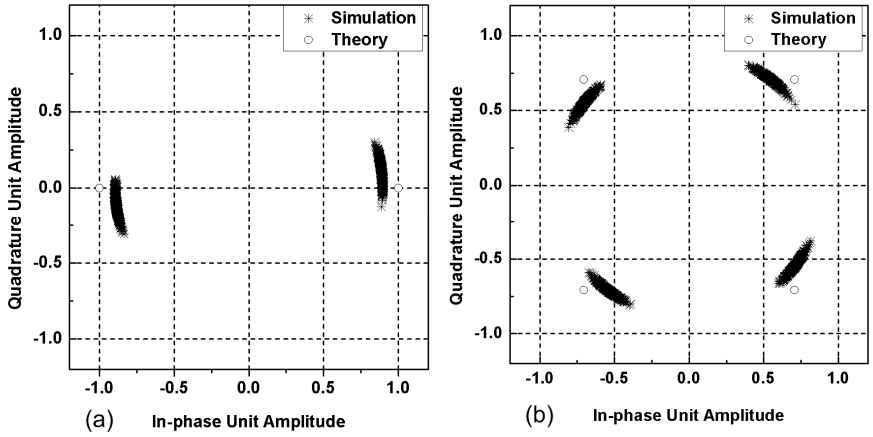

Figure 2.10: (a) BPSK constellation diagram; (b) QPSK constellation diagram.

From Table 2.3, the receiver noise floor can be calculated using $10\log_{10}(kT)+10\log_{10}(BW)+NF$ = -71.26 dBm. A minimum received power level of -59.26 dBm is sufficient to demodulate a BPSK modulated signal if a SNR of 12 dB is required for a BER of 1E-08. In low-order PSK modulations, such as BPSK, and QPSK, angle modulation, comprised of carrier frequency and phase, are more invulnerable to noise and interference, compared to other modulation schemes. Therefore, the millimeter-wave circuit nonidealities should not significantly impact the performance of BPSK or

QPSK. However, moving into higher-order constellations, SNR and phase noise due to oscillators become issues and degrade the sensitivity of a receiver drastically.

2.4.4 Quadrature Amplitude Modulation

Three different parameters are useful in modulating baseband signal: amplitude, carrier frequency, and phase. Quadrature amplitude modulation (QAM) combines both amplitude and angle (frequency and phase) to modulate baseband signals [45]. Unlike QPSK, QAM achieves higher spectral efficiency at the expense of higher circuit performance requirements, which directly conflicts the aforementioned emphasis of low-power and high-speed 60 GHz CMOS operation.

A 16 QAM modulation scheme encodes four bits per symbol, but it requires a SNR of 16 dB at the slicer to achieve a BER of 1E-08. This is an additional 4 dB SNR penalty compared to BPSK or QPSK, which implies that more bits are required by the baseband signal processor. Since the modulated signal is no longer a constant envelope, the PA linearity is challenged. Similar to the 16 PSK case, QAM is much more sensitive to the rotational symbol jitter caused by oscillator's phase noise due to closely-spaced constellation symbols.

In Figure 2.11(b), a simulation of 16 QAM signal space is performed incorporating PA nonidealities, LO phase noise, and AWGN effect. The penalty of the PA distortions is evident from the reduced amplitude. As can be seen, there are no constellation points found in coordinates (1, 1), (-1, 1), (-1, -1), and (1, -1). The output

constellation is heavily corrupted as the individual constellation points can no longer be distinguished, indicating an unacceptably high BER.

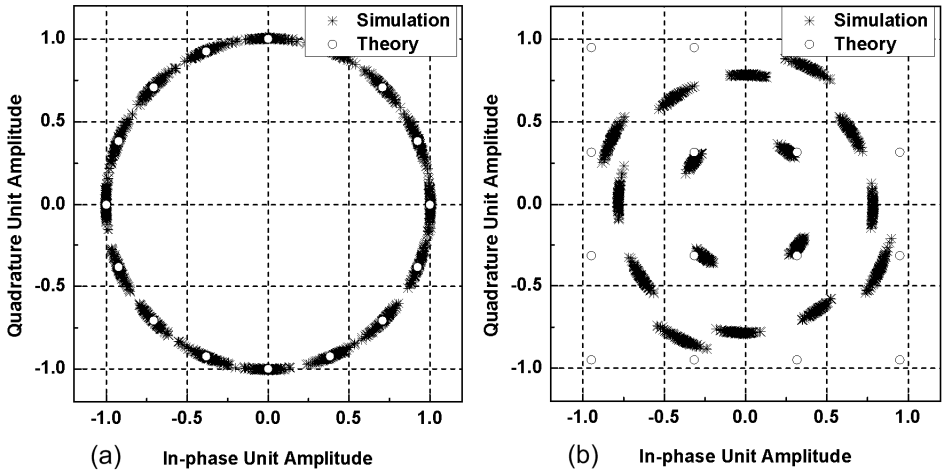

Figure 2.11: (a) 16 PSK constellation diagram; (b) 16 QAM constellation diagram.

2.4.5 Orthogonal Frequency-Division Multiplexing

Multi-carrier systems, such as OFDM, are popular demodulator architecture that has been used in several commercial wireless communications systems, such as 802.11a/g, MB-UWB, and 4G (WiMAX and LTE). The primary advantage of OFDM is its robustness to multipath by using a large number of closely-spaced, narrow-band orthogonal sub-carriers. The low symbol rate of sub-carriers has relatively longer delay spread; hence OFDM is able to cope with severe channel conditions, such as high-frequency attenuation in long copper wire, narrow-band interference, and multipath effects. The low-bandwidth sub-carriers also enable the use of guard interval that can

easily remove any intersymbol interference. Also, coding across sub-carriers enables the system to perform robustly in the presence of deep channel fades. The aforementioned advantages are attractive to NLOS environment, where space is heavily clustered with other existing wireless standards.

Figure 2.12 shows the block diagram of a generic multi-carrier OFDM demodulator. In the transmitter, the original serial data is divided into parallel channels by a serial-to-parallel converter, operating at lower data rate. Using the inverse fast Fourier transform (IFFT), the time-domain parallel channels are modulated by BPSK, QPSK, or 16 QAM before converting into frequency-domain channels. Then, they are transmitted simultaneously using 2^N orthogonal frequency carriers. In the receiver, the DSP performs fast Fourier transform (FFT) to transform the frequency-domain signals to time-domain. The Viterbi algorithm is used for decoding the data stream that has been encoded using forward error correction.

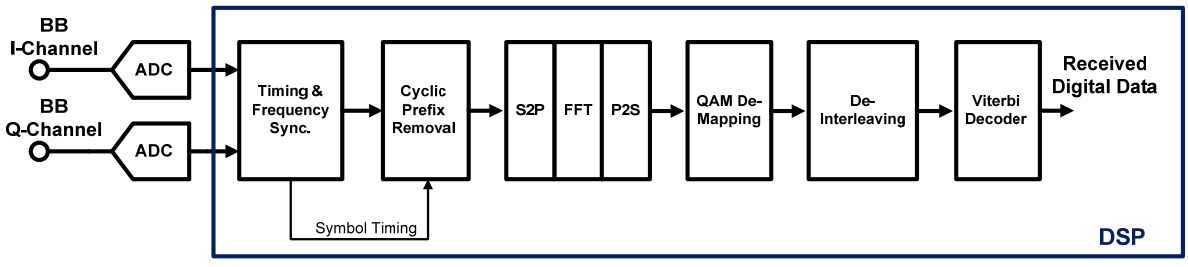

Figure 2.12: Block diagram of a generic multi-carrier OFDM demodulator system.

The use of multiple sub-carriers imposes significant performance constraints on the millimeter-wave circuitry. Figure 2.13 shows the simulated constellation diagrams of OFDM-QPSK and OFDM-16 QAM, respectively. The effects of PA nonidealities and a noisy channel are considered here. Unlike like the constellation diagram of OFDM-16 QAM, the constellation cloud is discernible for OFDM-QPSK and an error-free demodulation can still be maintained. On the other hand, the simulated BER for Figure 2.13(b) is only 6.4E-03, which is not sufficient for uncompressed HDMI video streaming.

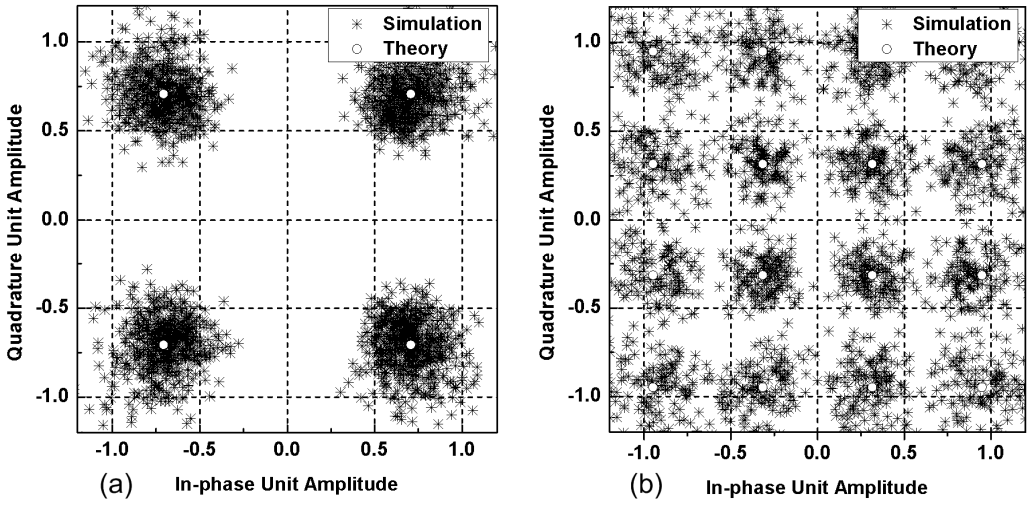

Figure 2.13: (a) OFDM-QPSK constellation diagram; (b) OFDM-16 QAM constellation diagram.

Increased power consumption and system complexity are the dominant issues when scaling the same architecture into multi-gigabit operations. [46] discusses the challenges of OFDM high-rate systems targeting for UWB applications at a sampling rate of 1.058 GHz. Based on the IEEE P802.15 multi-band OFDM physical layer proposal for

WPANs, several companies have studied the complexity of 90 nm CMOS FFT and Viterbi cores for the multi-band OFDM. For example, Philips estimated that a 90 nm CMOS FFT core of 64 K gates and a Viterbi decoder of 100 K gates operating at 480 Mbps are likely to consume 50.7 mW and 79 mW, respectively. Operating OFDM systems at multi-gigabit is inevitably going to consume hundreds of milliwatts. Therefore, given the performance of millimeter-wave CMOS front-end components and the magnitude of system complexity, an OFDM system based receiver is not suitable for high-capacity multi-gigabit applications due to high-resolution data converters and linearity requirements.

2.5 Summary

From Section 2.2, the most suitable technology for millimeter-wave communications systems is the 60 GHz band based on the requirements for short-distance high-speed wireless applications. Using heterodyne architecture, issues, such as flicker noise, and DC offset, can be alleviated significantly, and the receiver sensitivity is enhanced greatly. Based on achievable output power, gain, and noise figure, the state-of-the-art CMOS front-end components are also evaluated. Knowing the CMOS performance limitations, low-order PSK and ASK modulated signals are more suitable to satisfy the requirements of low-cost, multi-gigabit, and wireless applications.

Figure 2.14 shows the theoretical BER versus SNR for various modulation schemes. One can easily show that BPSK and QPSK require least SNR to achieve a BER

of 1E-08 compared with ASK, 16 QAM, and 16 PSK. Low-order PSK modulation schemes are more efficient in terms of the occupied bandwidth and the transmitted power. On the other hand, high-order PSK, such as 16 PSK, is extremely sensitive to LO phase noise. Although ASK utilizes the simplest circuit components to recover data, the receiver sensitivity suffers greatly and is vulnerable to interferences. Furthermore, 16 QAM modulated signal is not a constant envelope, and its constellation can be easily distorted due to PA and LO nonidealities. The high PAR and system complexity impose stringent requirements for the OFDM systems. This makes it difficult to implement even using advanced CMOS process.

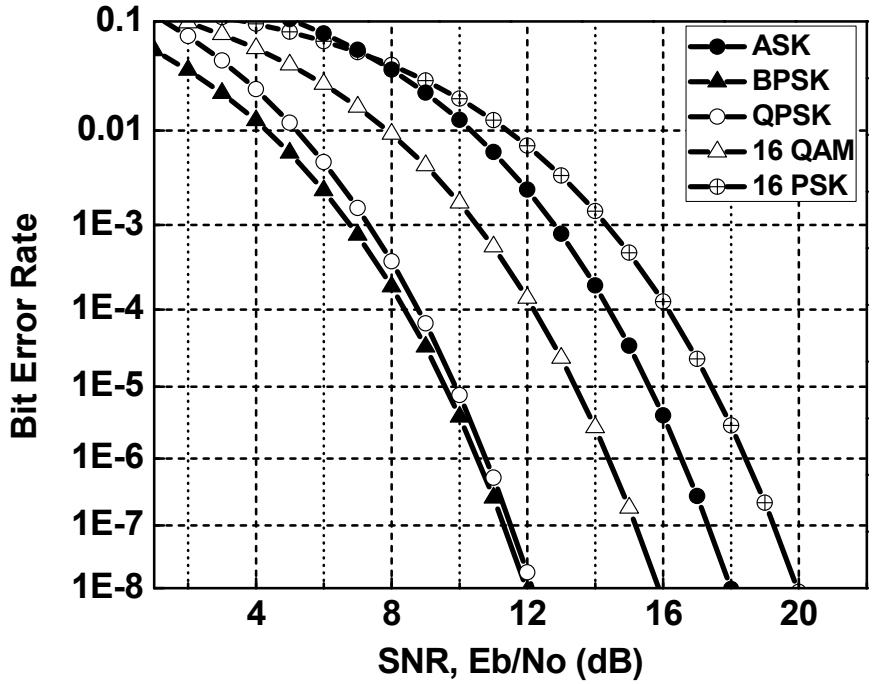

Figure 2.14: BER versus SNR for various modulation schemes.

Table 2.6 compares and summarizes the modulation schemes in terms of the required SNR for a BER of 1E-08, estimated PAR, PA linearity, phase noise requirement, and ADC resolution. The remaining chapters of this dissertation focus and demonstrate a practical system platform to realize a portable, robust, low-cost, low-power, high-speed demodulator system in 90 nm CMOS technology.

Table 2.6: Summary of modulation schemes.

Specifications	BPSK	QPSK	16 QAM	16 PSK	OFDM-QPSK
SNR (BER = 1E-08)	12 dB	12.15 dB	16 dB	20 dB	12 dB
PAR	Low	Low	Med	Med	High
PA linearity	Low	Low	Med	Low	High
Phase noise requirement	Low	Med	High	High	High
ADC resolution	3 bit	4 bit	6 bit	8 bit	6 bit

CHAPTER 3

ANALOG-TO-DIGITAL CONVERTERS

3.1 Introduction

The aggressive scaling of CMOS technology changes the landscape of high-speed ADCs. Fast and efficient ADCs are a key to enabling powerful DSPs for various signal conditioning and modulations. As seen in [47], [48], [49], the state-of-the-art CMOS ADCs have demonstrated significant improvement in power and area efficiency for small resolution at low gigahertz conversion rates using deep sub-micron CMOS process. This chapter discusses the practical high-speed ADC architectures for large wireless system-on-chip (SOC) integration. Fundamental limits to high-speed performance are next described. Finally, a review of the state-of-the-art CMOS ADCs is compared and evaluated based on a universal figure of merit (FOM).

3.2 High-Speed ADC Architectures

ADCs range from the oversampling delta-sigma to medium-speed successive approximation register (SAR) and to the highest sampling speed, flash. Among those types of converters, flash converters are the most standard approach for realizing very-high-speed applications [47], [50], [51], [52], [53], [80]. Moreover, flash ADCs guarantee the fewest clock cycles per conversion and thus the minimum latency. Another popular

architecture based on interpolation is also discussed. Although interpolation technique does not guarantee the same linearity and accuracy in the flash design, its input capacitance can be reduced greatly at higher resolution

3.2.1 Full Parallel (Flash) ADC

Figure 3.1 shows the block diagram of an *n*-bit flash ADC. The input to the flash ADC is an analog signal and its output is binary. The design involves mixed-signal techniques and consists of two elements: analog and digital. The analog design includes a front-end track-and-hold (T/H) circuit, voltage references comprising 2^N-1 equal segments, 2^N-1 preamplifiers, 2^N-1 comparators, and 2^N-1 latches. The voltage reference can be generated using resistor ladders, current-steering circuits, or switched-capacitor circuits. The preamplifiers first sense and amplify the difference between sampled analog input with these voltages. For example, if the analog voltage, V_{in}, is between V_{r1} and V_{r2}, the sign of first preamplifier's output should be positive, and the rest are negative. The job of comparators then is to saturate this difference to supply voltage, and the comparator functions as a nonlinear amplifier. In other words, the comparator output of V_{r1} should produce a logic one while the rest remain zero. As a result, this output behavior constitutes a thermometer code. In low-frequency applications, the preamplifiers stage in Figure 3.1 may be removed to save power. The digital design includes error correction and various types of encoding schemes. At multi-gigahertz sampling rates, the digital design requires special treatments by exploiting ASIC design flow. Detailed implementation is discussed in the next chapter.

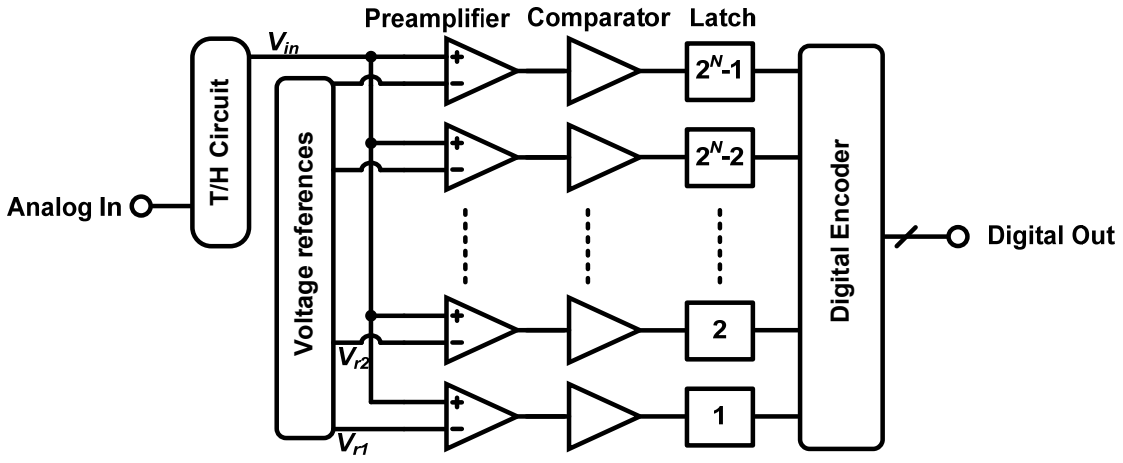

Figure 3.1: Block diagram of an *n*-bit flash ADC.

In absence of T/H circuit, the ADC input directly loads with 2^N-1 preamplifiers, degrading the input bandwidth. Unless the preamplifiers are designed to have high regenerative gain and large bandwidth at the expense of higher power consumption, time-dependent jitters and noise impact the linearity performance of ADC. Therefore, front-end T/H circuit is the most critical component and demands good linearity at high sampling rates. Since the comparators are nonlinear amplifiers, higher speeds can be achieved compared to the T/H circuit. In addition, preamplifiers, comparators, and latches often incorporate clocked switch transistors to improve regenerative time constant [50]. The clocked regenerative feature also acts as a polarity sampling amplifier. By operating these amplifiers in the amplification mode during the first half cycle, the difference at the input can be instantaneously latched to a logic level in the next cycle. This timing arrangement allows higher speed and higher gain.

For higher resolution at high sampling rates, flash converters suffer from three major drawbacks. First, the exponential growth of area, power consumption, and input capacitance prohibits flash architecture from being implemented at 8-bit or higher. For example, an 8-bit flash ADC requires 255 comparators. Second, the presence of comparator offsets due to devices mismatch is difficult to cancel since there are 255 of them at 8-bit resolution. Last, the linearity of the input T/H circuit limits the accuracy to about 8-bit in low supply voltage.

3.2.2 Interpolating ADC

A close family of flash ADC is the interpolating converter. The block diagram of an *n*-bit interpolating ADC is shown in Figure 3.2. Unlike the full-parallel ADC, an *n*-bit interpolating ADC only uses 2^{n-1} preamplifier for an interpolating factor of two, but the number of comparators and latches remains the same. The components labelled in gray color represent the interpolated path. This technique reduces the input capacitance of preamplifiers greatly. For example, a 4-bit interpolating ADC uses only eight input preamplifiers with their voltage references spaced two LSBs apart. By interpolating between the adjacent outputs, additional seven more signals are obtained and can be seen as virtual preamplifier outputs for the other seven levels that were skipped. This method reduces the effective input capacitance by half because the number of preamplifiers decreases from fifteen to eight. In addition, the requirement of accurate reference voltage is relaxed since fewer numbers of reference voltages are needed.

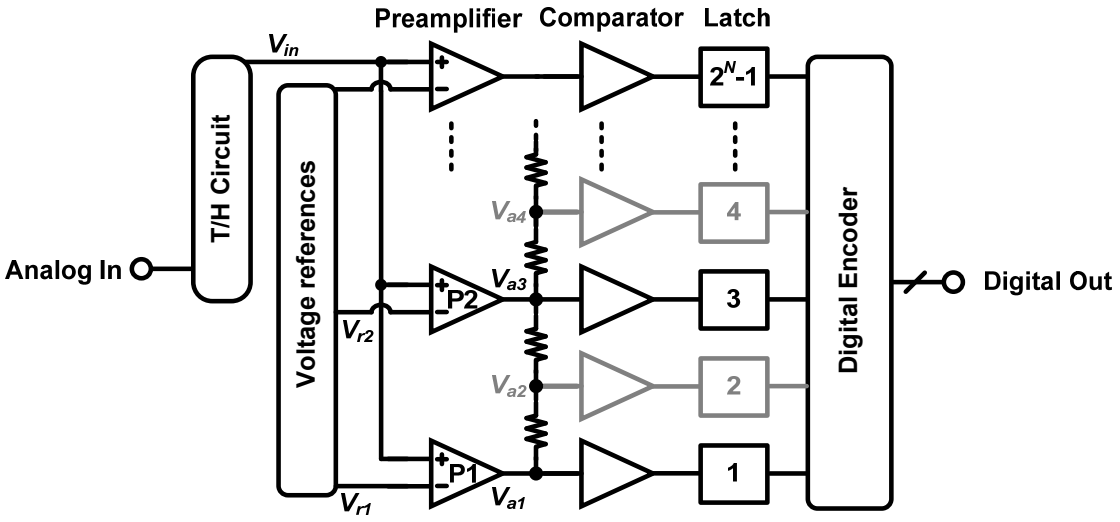

Figure 3.2: Block diagram of an *n*-bit interpolating ADC.

To further understand this architecture, the interpolated and amplified signals are shown in Figure 3.3. Preamplifiers P_1 and P_2 compare the analog input, V_{in}, with V_{r1} and V_{r2}, and the outputs are shorted by two series resistors. Assuming zero offset for both preamplifiers, an interpolated zero-crossing is created at $V_{in} = (V_{r1} + V_{r2}) / 2$, and the interpolated output is labeled V_{a2}. When the resistance or the output impedance at the interpolated nodes is loaded with significant capacitance, additional delay could degrade the overall linearity of ADC, especially at high frequencies. To overcome this issue, preamplifiers should be designed to have sufficient driving capability to the interpolated resistor chain. If the output impedance of preamplifiers is small compared to the interpolated resistor, then no interaction between the stages occurs. As the number of interpolation factor increases, extra delay introduced in the middle nodes becomes

impractical for high-frequency applications. However, an interesting property that accompanies interpolation technique is the improved differential nonlinearity (DNL) caused by the input offset voltage of the differential preamplifiers [54].

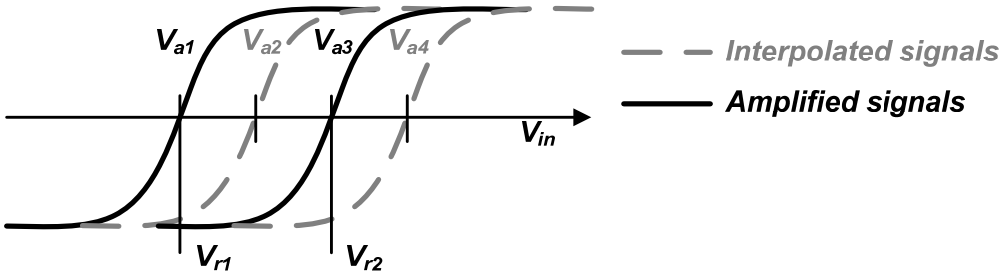

Figure 3.3: Outputs and interpolated responses.

3.2.3 ADC Architectures Comparison

Table 3.1 compares the existing ADC architectures based on speed, power consumption, area, and latency. To realize the highest sampling ADC, full-parallel architecture is the best candidate only when small number of resolution is desired. At the same time, low power consumption can be maintained [47]. This implies that a robust modulation scheme to go with small-resolution high-speed ADC is the constant envelope single-carrier PSK family.

Table 3.1: ADC architectures comparison.

Architecture	Advantages	Disadvantages
Full-parallel (Flash)	• The fastest • Low latency • Basically monotonic • No DAC required	• Exponential power increase • Limited input dynamic range • High input capacitance
Interpolating	• High speed • Basically monotonic • Lower input capacitance compared to flash	• Worse linearity compared to flash • Limited input dynamic range • High power consumption
Two-step	• Moderate transistor count • Low input capacitance	• Moderate sampling rate • Moderate latency
Pipelined	• Highest throughput • Error correction possible • Low input capacitance	• Multiple T/H circuits required • Moderate power consumption • Moderate latency
SAR	• Lowest power consumption • Low input capacitance	• Highest latency • Low sampling rate

3.3 Fundamental Limits to Performance

3.3.1 Periodic Sampling

ADCs generally require more power and circuit-level complexity than DACs to achieve a given speed and resolution. An ADC converts a continuous quantity to a discrete digital code by means of analog signal processing to digital sampling. This sampling process is the most important attribute in analog-to-digital conversion. Traditionally, ADCs are used in instrumentation testing and signal processing applications, where the time-domain performance is more significant than the frequency-domain performance. However, the availability of broadband millimeter-wave communication channels requires gigahertz sampling ADCs. As a result, the dynamic specifications have been gaining more attention recently.

One of the most important theorems concerning the sampling process is called the Nyquist criterion [3]. Figure 3.4(a) shows a continuous-time signal, which is sampled periodically ($T_s = 1/f_{clk}$). Its corresponding frequency-domain representation is shown in Figure 3.4(b). The sampling process can be classified into three types: oversampling, undersampling, and Nyquist sampling. In terms of Nyquist zones, if and only if the frequency of the input signal, f_{in}, falls inside the first Nyquist zone, the sampling process is defined as oversampling. Otherwise, the sampling process is considered undersampling. When f_{in} is just half of f_{clk}, the sampling process is called Nyquist sampling. Theoretically, the entire information contained in the first Nyquist zone is sufficient to recover the original signal. Therefore, a low-pass filter (LPF) is normally implemented up to 0.5 f_{clk} to reject unwanted interferences due to aliases or images, f_{image}.

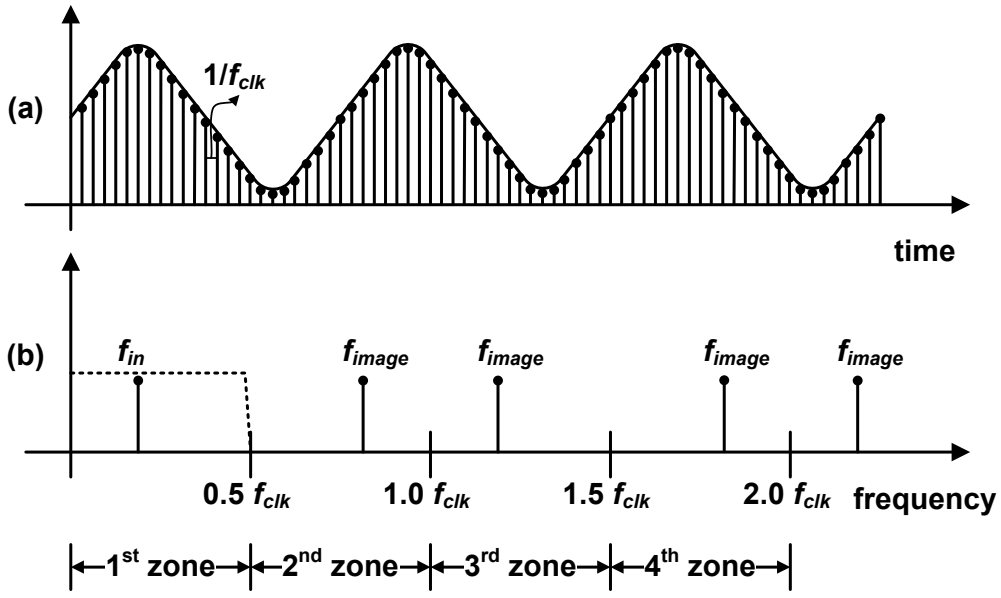

Figure 3.4: (a) A sampled signal in time-domain; (b) A sampled signal in frequency-domain.

The sampling process can be further understood mathematically using the model in Figure 3.5. The time-domain input signal has the form:

$$x(t) = V_p \cos(2\pi f_{in} \cdot t), \tag{3.1}$$

where V_p is the peak amplitude in volts, and f_{in} is the input frequency in hertz. The sampled output signal, *y(t)*, is generated by multiplying the input signal, *x(t)*, with a periodic impulse train, $\delta(t-nT_s)$, which can be expressed as

$$y(t) = \sum_{n=-\infty}^{\infty} V_p \cos(2\pi f_{in} \cdot t) \cdot \delta(t - nT_s), \tag{3.2}$$

where T_s is equal to the inverse of sampling frequency, and *n* is the integer index number. The normalized frequency spectrum of the sampled output is already shown in Figure 3.4(b). (3.2) can be expressed in frequency-domain using Fourier transform:

$$Y(f) = \frac{V_p}{2T_s} \sum_{n=-\infty}^{\infty} [\delta(f - f_{in} - nf_s) + \delta(f + f_{in} - nf_s)], \tag{3.3}$$

where *Y(f)* is expressed in frequency. The term nf_s indicates that images or replicas are introduced at every *nth* sampling frequency within a plus and a minus of f_{in}. The exact positioning of aliases for one-sided spectrum can be expressed as

$$nf_s \pm f_{in}, \tag{3.4}$$

where *n = 1, 2, 3, 4...* . If an ideal LPF is applied to the output spectrum of the sampler with a bandwidth just greater than f_{in}, then the higher-order frequency components can be removed completely as expected.

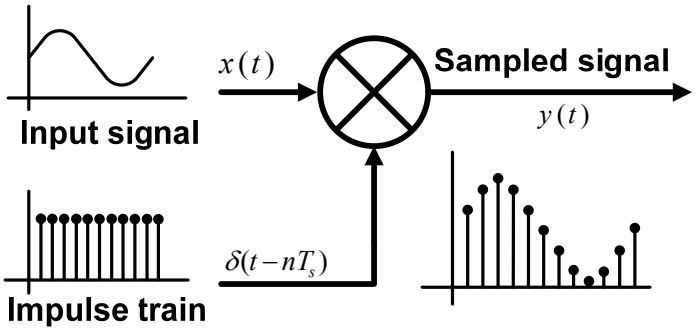

Figure 3.5: Impulse sampling model.

3.3.2 Quantization Noise

When an analog signal goes through the sampling process, the quantization error becomes an unavoidable fundamental limit to SNR. When the number of bits goes to infinity (the ideal case), the quantization error contributes zero noise. The quantization noise can be treated as a random variable, ε_Q, falling in the range of ±0.5 least significant bit (LSB) [55]. Then, the quantization error can be derived by assuming a constant probability density function, $p(\varepsilon_Q)$, in the range of -0.5 LSB to +0.5 LSB, and outside this range, $p(\varepsilon_Q)$ is zero. Therefore, the time average power of the quantization error, P_{QE}, is given by

$$P_{QE} = \int_{-0.5LSB}^{0.5LSB} \frac{\varepsilon_Q^2}{LSB} \cdot \partial\varepsilon_Q = \frac{LSB^2}{12}, \tag{3.5}$$

where P_{QE} is expressed in volts squared rather than watts. If the input to the ADC is a sine wave, then the average power of this sine wave can be expressed in terms of LSB:

$$P_{\sin} = \frac{1}{\pi}\int_0^{\pi} V_p^2 \cdot \sin^2(t) \cdot \partial t = \frac{V_p^2}{2} = \frac{LSB^2 \cdot 2^{2n}}{2 \cdot 4}, \tag{3.6}$$

where V_p is the peak amplitude in volts, and n is the number of bits. The SNR of ADC in logarithmic decibel scale is defined as the power ratio between the sine wave and the quantization noise from (3.5) and (3.6):

$$SNR_{ADC} = 10\log(\frac{P_{\sin}}{P_{QE}}) = 10\log(\frac{3}{2}) + 10\log(2^{2n}) = 1.76 + 6.02 \cdot n. \tag{3.7}$$

The key understanding here is that for every additional bit of resolution, the SNR improves by 6.02 dB. For low-resolution ADCs, this fundamental SNR relation limits the use of higher-order modulation schemes. In practice, data converters are never ideal, and the output spectrum contains distortion noises other than the quantization noise. Therefore, (3.7) can be modified considering undesired harmonic distortions and other noise sources in the system:

$$ENOB_{ADC} = \frac{SNDR - 1.76}{6.02}, \tag{3.8}$$

where *ENOB* is the effective number of bit, and *SNDR* is the signal-to-noise plus distortion ratio in dB.

3.3.3 Thermal Noise

Although the quantization noise is inherent in the sampling process, thermal noise is another fundamental limit to performance caused by the random thermally excited vibration of the charge carriers in a conductor. For example, the noise spectrum of a resistor is white in the band of interest and is given by

$$S_R(f) = 4kTR, \tag{3.9}$$

where $S_R(f)$ is expressed in volts squared per root Hertz, k = 1.38E-23 is the Boltzmann constant in J/K, T is the temperature in Kelvin, R is the resistor value in Ω, and f is the frequency of interest and should be greater than zero for one-sided spectral density.

Figure 3.6(a) shows the schematic of a simple T/H circuit, consisted of a *NMOS* transistor and a capacitor. When the gate voltage of transistor M_1 is high, this circuit tracks the input voltage. To simplify analysis, when the transistor is on, it is modeled as a resistor in deep triode operation. Otherwise, the transistor turns off, and the sampled voltage is held by the capacitor. The resistor and capacitor generate thermal noises and form a low-pass filter at V_{out}. Using the noise equivalent circuit model, as shown in Figure 3.6(b), the total noise power due to thermal noise can be expressed as

$$P_{TN} = \int_0^\infty S_R(f) \cdot \left| \frac{1}{1 + j2\pi RCf} \right| \cdot \partial f = \int_0^\infty \frac{4kTR}{1 + (2\pi RCf)^2} \cdot \partial f = \frac{kT}{C}, \tag{3.10}$$

where P_{TN} is expressed in volts squared rather than watts, $S_R(f)$ is the noise spectral density of a resistor, R is the equivalent resistance of *NMOS* transistor in deep triode

region, and C is the sampling capacitor. (3.10) implies that the noise power of T/H circuit does not depend on the resistor value. Although increasing the resistance raises the white noise floor, the corner frequency formed by the RC is also enhanced. This means that the R dependency is cancelled through these two effects, and the noise power becomes only a function of the capacitor. Therefore, kT/C becomes the fundamental limit to the front-end T/H circuit design in CMOS ADCs.

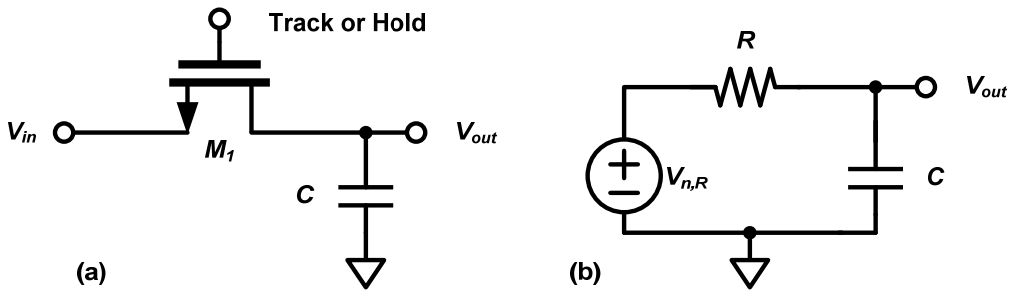

Figure 3.6: (a) T/H circuit schematic; (b) Noise equivalent circuit.

The quantization noise and thermal noises can be modelled as two uncorrelated noise sources in the signal path. Figure 3.7 shows the simulated SNDR due to these noise sources at various sampling capacitor values. The full-scale input dynamic range is specified as 640 mVpp. When the sampling capacitance is 50 fF only, the simulated SNDR flattens out after 8-bit resolution, indicating a limit due to the thermal noise.

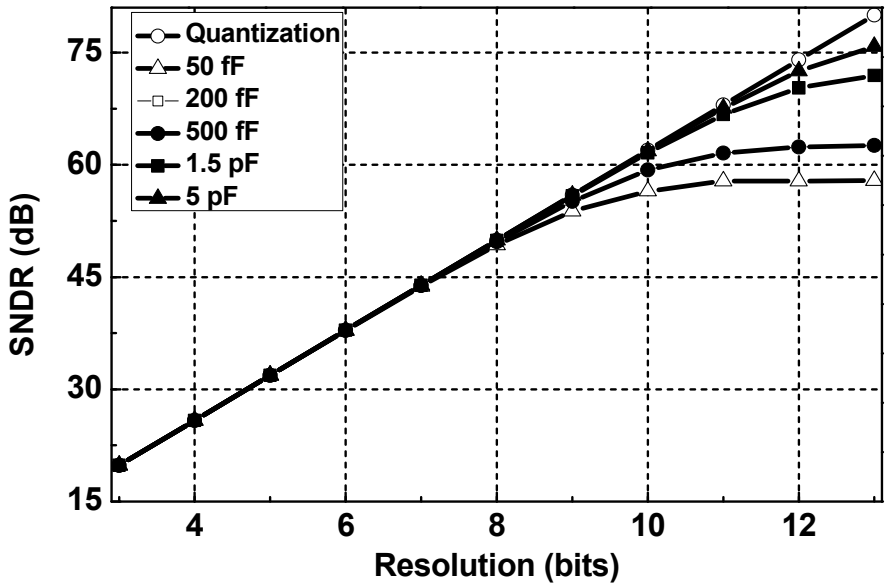

Figure 3.7: Simulated SNDR considering quantization and thermal noises.

3.3.4 Aperture Jitter

Thermal noise due to a sampling capacitor is the fundamental limit when high-resolution converters are desired. However, at high operating frequencies, the sampled data encounters sampling-time errors caused by the uncertainty of clock signal, known as the aperture jitter [56]. Figure 3.8 shows an example when an input signal is sampled under clock jitter, $\Delta\delta$. The sampling uncertainty displays a spread of variation in seconds that causes an amplitude variation at the output, ΔX. The sampling error due to clock jitter can be expressed as

$$\Delta X(t) = X_{in}^{'}(t) \cdot \Delta\delta, \tag{3.11}$$

where $X'_{in}(t)$ is the derivatives of input signal, and $\Delta\delta$ is the clock jitter. If the input is a cosine wave with amplitude, V_p, then the sampling error can be simplified to

$$\Delta X(t) = -V_p \cdot \omega_{in} \cdot \sin(\omega_{in} \cdot t) \cdot \Delta\delta\,, \tag{3.12}$$

where V_p is the peak amplitude in volts, and ω_{in} is the input angular frequency in radians per second. Since the clock jitter is assumed to be a random variable with white spectrum, the cosine modulation has no effect on white spectrum. The time average noise power caused by sampling error can be shown:

$$P_{JI} = \frac{1}{T_s}\int_0^{T_s} (-V_p \cdot \omega_{in} \cdot \Delta\delta)^2 \cdot \sin^2(\omega_{in} \cdot t) \cdot \partial t = \frac{V_p^2 \cdot \omega_{in}^2 \cdot \Delta\delta^2}{2}\,, \tag{3.13}$$

where P_{JI} is expressed in volts squared rather than watts.

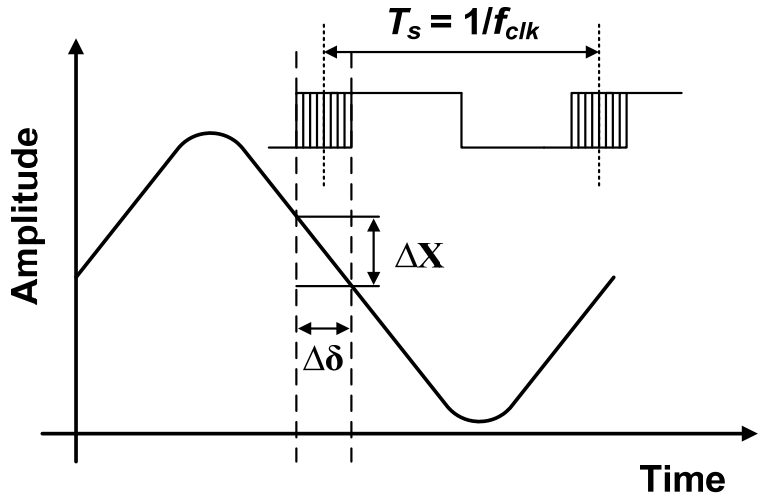

Figure 3.8: Diagram of input signal and sampling uncertainty.

Unlike the quantization error or thermal noise, the sampling error is a function of input frequency and clock jitter. As the input frequency reaches multi-gigahertz regime, the required clock jitter is less than a few picoseconds. Table 3.2 summaries the parameters used to simulate SNDR with nonidealities. Three noise sources, including quantization noise, thermal noise, and aperture jitter, are considered, and each noise power is added linearly assuming uncorrelated noises. Then, the SNDR can be computed by taking the ratio between the time average input signal power and the sum of these noise sources.

Table 3.2: Parameters for the SNDR simulation.

Specification	Parameter	Unit
Full-scale range	640	mVpp
Boltzmann constant	1.38E-23	J/K
Temperature	300	K
Resistor	200	Ω
Capacitor	150	fF
T/H circuit bandwidth	5.3	GHz
Input frequency	2	GHz

The SNDR degradation due to additional sampling error is observed in Figure 3.9. The slope is linear considering only the quantization noise, and the *kT/C* thermal noise limits SNDR to around 9-bit resolution. Unlike those two cases, the clock jitter impacts SNDR more severely. For example, when a clock jitter of 5 ps is considered in addition to quantization noise and thermal noise, the SNDR saturates after 4-bit resolution. To achieve an ENOB of 6-bit, the clock jitter should be small than 1 ps. When a higher-order

modulation scheme, such as 16 QAM, is chosen, not only does the design of high-speed ADC become stringent, the required performance of baseband frequency synthesizer is also challenged.

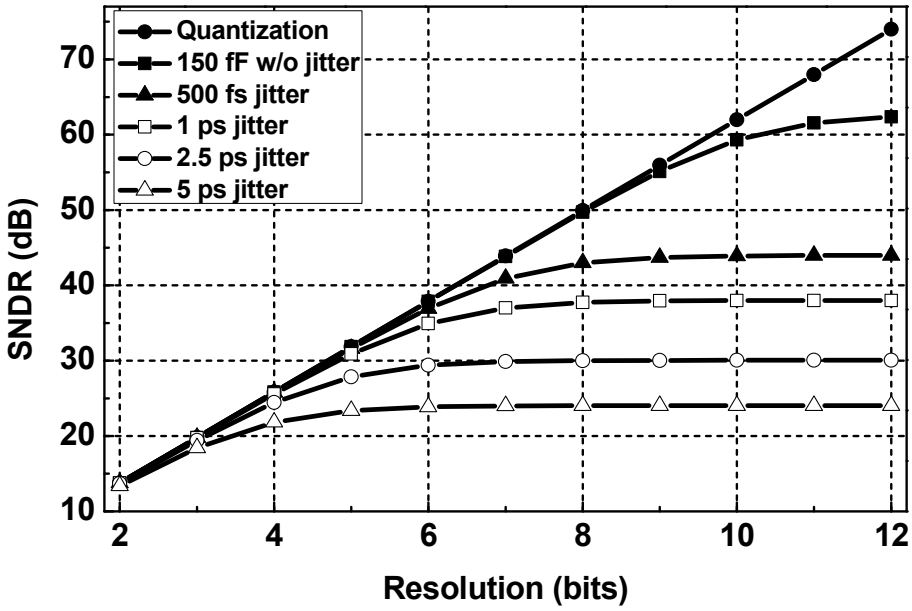

Figure 3.9: Simulated SNDR considering quantization noise, thermal noise, and clock jitter.

3.3.5 Comparator Design Consideration

Comparator offset and regenerative time place a vital fundamental limit on achievable resolution [57], [58], [59], [60]. As seen in (1.4), the comparator offset directly introduces DNL errors and possibly causes non-monotonicity. This occurs when the trip-points of adjacent comparators are interchanged. As a result, bubble, sparkle, or

metastability errors are produced in the output thermometer codes that increase the noise power in quantizer output waveform.

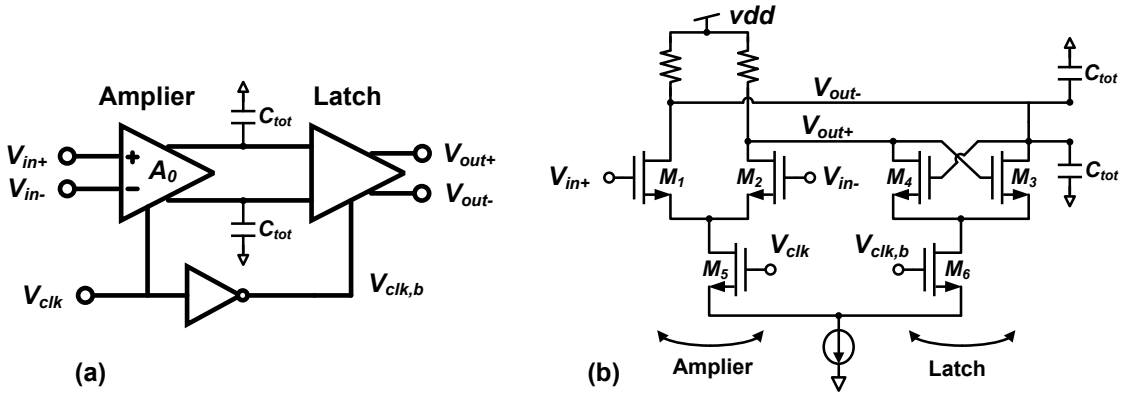

Figure 3.10: (a) Comparator functional diagram; (b) Comparator schematic.

Unlike the comparator offset voltage, comparator regenerative time constant is associated with the frequency response. Figure 3.10(a) shows the functional diagram of a comparator often utilized in ADCs. It consists of a differential amplifier stage with a voltage gain of A_0 followed by a latch. Between the amplifier output and latch input, a shunt capacitance, C_{tot}, represents the equivalent capacitance, including interconnects parasitics, gate-to-source capacitance, C_{gs}, and gate-to-drain capacitance, C_{gd}. An example of transistor-level schematic is shown in Figure 3.10(b). When V_{clk} is high, the comparator tracks input voltage and amplifies the difference. In latching mode ($V_{clk,b}$ = 1), the input differential pair is switched off, and the latch pair, M_4-M_5, is enabled. The instantaneous output of comparator is regeneratively amplified by means of positive

feedback, and logic level is produced at V_{out}. Together the tracking and latching modes complete a clock cycle.

If the comparator is not given a sufficient time to produce a logic-level output, then for some range of differential input value near zero, the comparator output will not interpret properly. This logic can potentially produce bubble, sparkle, or metastability errors. Assuming the resistance of comparator load is much larger than the transconductance of M_4-M_5, the regenerative time constant is expressed:

$$\tau_L = \frac{C_{tot}}{gm_{M4-M5}}, \tag{3.14}$$

where C_{tot} is the total capacitance at the amplifier output, and gm_{M4-M5} is the transconductance of the latch pair. The metastability error probability can be approximated to the first order by

$$P_{PE} = \frac{V_{out}}{V_{in} \cdot A_0} e^{-t_L/\tau_r}, \tag{3.15}$$

where V_{out} is the output voltage swing required for valid logic levels, t_L is the latch phase period, τ_r is the regenerative time constant, V_{in} is the input swing, and A_0 is the amplifier gain [56], [61]. Typically, the latch phase is half of a clock period. The metastability error increases exponentially with reduced period. To overcome metastability errors, the comparator is usually designed to drive a small differential input value less than half LSB.

3.3.6 Capacitive Loading and Resistor Bowing

Given a fixed supply voltage, higher ADC resolution requires a large number of comparators and smaller offset voltage at the input node by choosing input transistors size large. Larger capacitance is then present at the flash ADC input, which degrades the bandwidth and increases the driver power consumption. Two challenges occur at high speed that could potentially distort the linearity: input capacitive loading and resistor string bowing. Figure 3.11 shows the schematic of a preamplifier, where the input pair is connected to a voltage source and a resistor ladder, respectively.

First, the input signal loss error is observed due to the input capacitive loading, mainly the C_{gs} of transistors M_1-M_2. This error is given by

$$\frac{V_g}{V_{in}} = \frac{2 + s \cdot R_{eq} \cdot C_{gs}}{2 + s \cdot (R_{in} + R_{eq}) \cdot C_{gs}}, \tag{3.14}$$

where R_{in} is the input resistance, and R_{eq} is the equivalent resistance of the ladder network. Maximum error occurs when R_{eq} is equal to $R \cdot 2^{n-1}$, where n is the number of resolution. At high frequencies, resistor string bowing also becomes an issue and can be expressed as

$$\frac{V_{err}}{V_g} = \frac{s \cdot C_{gs} \cdot R_{eq}}{2 + s \cdot C_{gs} \cdot R_{eq}}, \tag{3.15}$$

where R_{eq} is as large as $R \cdot 2^{n-1}$. The input current through the transistor parasitic capacitance causes errors on the resistive voltage reference ladder. To minimize both signal loss error and bowing error, C_{gs} and R_{eq} should be minimized at the cost of

increased random offset mismatch and higher current flow. In Chapter 6, resistive averaging network will be introduced to minimize random offset voltage due to aggressive device scaling.

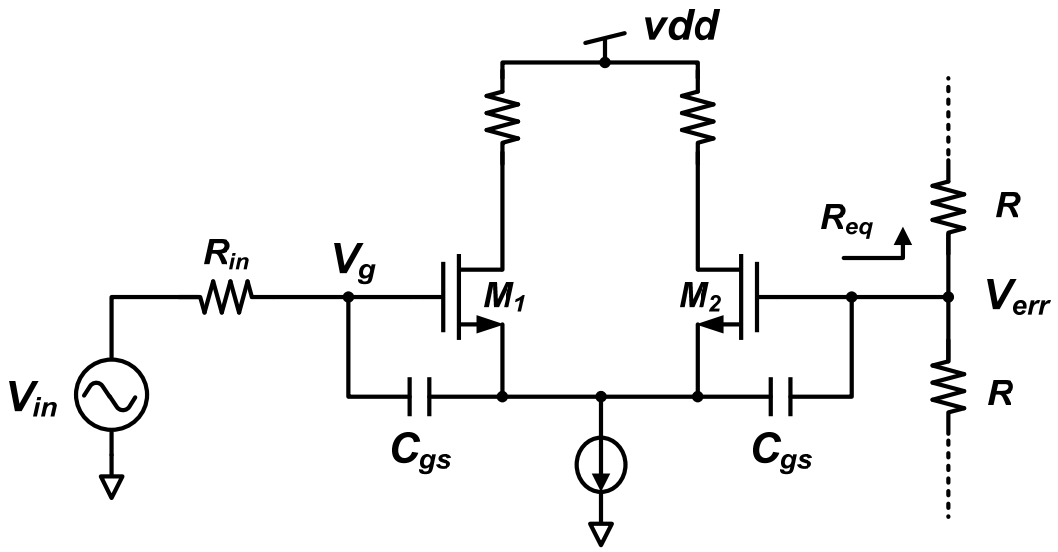

Figure 3.11: Preamplifier schematic with resistor string.

3.4 State-of-the-Art CMOS A/D Converters

This section surveys the state-of-the-art ADCs presented at *IEEE Solid-State Circuits Conference* (*ISSCC*) and *IEEE Symposium on Very-Large-Scale Integration (VLSI) Circuits*. Figure 3.12 shows a scatter plot of normalized ADC energy efficiencies from year 1997 to 2010 based on an empirically justified FOM given by

$$FOM_{ADC} = \frac{P}{2^{ENOB} \cdot f_{sample}}, \tag{3.16}$$

where P is the averaged power consumption in watts, *ENOB* is the effective number of bits, and f_{sample} is the maximum sampling rate in Hertz [62]. For a given flash ADC, every additional bit doubles the silicon area and power consumption. However, if the ENOB can increase linearly with every additional resolution, then the energy efficiency remains the same. Unfortunately, in reality, the complexity of the growing interconnects and various timing issues tend to deteriorate ENOB at higher frequencies. The state-of-the-art ADCs with energy efficiencies less than 10 pJ from 10 MS/s to 15 GS/s are considered in Figure 3.12.

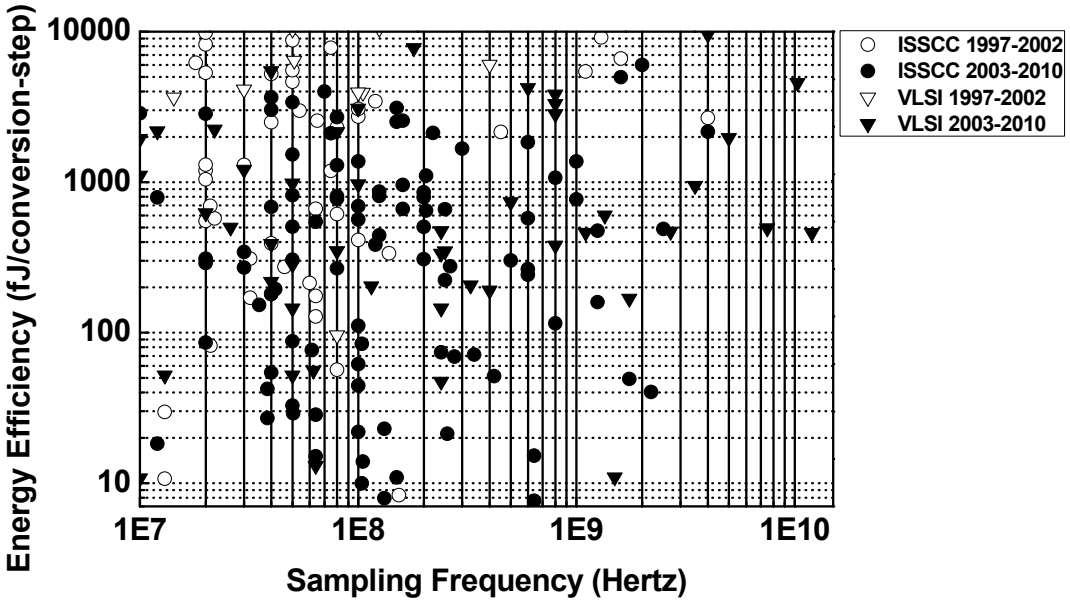

Figure 3.12: Energy efficiency of state-of-the-art ADCs.

The majority ADCs below 1 GS/s have demonstrated a very-good energy efficiency of 10 fJ or less. Beyond 3 GS/s, only two ADCs up to date have successfully

met the energy efficiency of 500 fJ [64], [65]. Their detailed performance summary is listed in Table 3.3. Although these state-of-the-arts ADCs achieve a sampling rate of 12 GS/s and 7.5 GS/s, respectively, the use of 1.1 V supply voltage in 65 nm CMOS technology is not justified, where the nominal supply voltage specified by the foundry is 1 V only. There are also two publications that meet low energy efficiency of 500 fJ at a sampling rate of 2.5 GS/s and 2.7 GS/s, respectively [63], [66].

Table 3.3: High-performance state-of-the-art ADCs.

Ref.	Technology (nm)	Supply (V)	Power (mW)	Sampling rate (GS/s)	ENOB (bit)	FOM (fJ/step)
[63]	45	1.1	50	2.5	5.4	480
[64]	65	1.1	81	12	3.88	460
[65]	65	1.1	52	7.5	3.8	497
[66]	90	1	50	2.7	5.3	470

In Figure 3.13, the comparison of state-of-the-art ADCs is further evaluated based on power consumption. Similar to the energy efficiency plot, the lower right corner is the target mainstream for future high-speed ADCs in deep sub-micron CMOS technologies. This pushes the ADCs to operate beyond a sampling rate of 3 GS/s at a power budget of 100 mW or less.

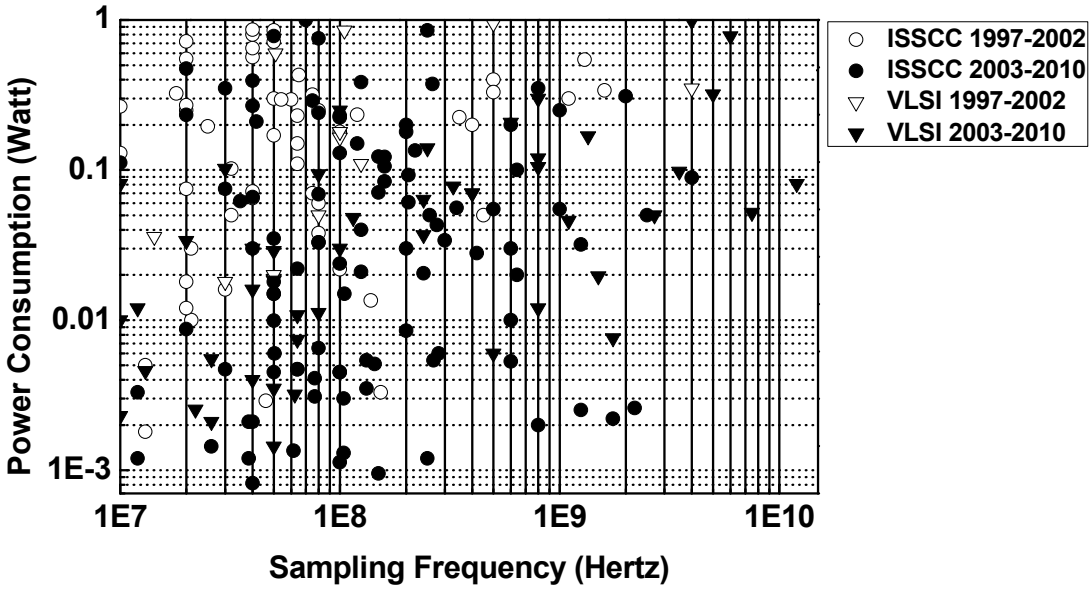

Figure 3.13: Power efficiency of state-of-the-art ADCs.

3.5 Summary

An ideal converter can be characterized by the following features:

- The only noise power caused by the sampling process is quantization level.
- The phase relation of clock and input analog signals at the sampling moment remains constant with respect to all amplifiers and comparators for any input or clock frequencies.
- The transistor threshold voltages are constant in all preamplifiers and comparators stages.

- There exists no data pulse width violations, no minimum period violations, and no minimum pulse width violation at gigahertz clock rates.

However, in real converters, dynamic effects cause deviations from these ideal conditions. Especially in deep sub-micron CMOS technologies, low supply voltage, noisy substrate, and devices variation become major issues in designing high-speed converters. Therefore, the following lists the counterparts to ideal cases:

- The *kT/C* thermal noise limits the linearity of T/H circuit to about 8/9-bit resolution.

- At multi-gigahertz sampling rates, aperture jitter impacts the SNDR significantly. At 2 GHz input frequency, a clock jitter of 5 ps limits the effective resolution to 4-bit.

- Devices mismatch is severe in deep sub-micron CMOS technologies. The random static offset voltage of CMOS circuits is a few millivolts.

- Due to the regenerative time constant and the associated bandwidth of amplifiers, bubble, sparkle, and metastability errors, create challenges in high frequencies.

CHAPTER 4

APPLICATION-SPECIFIC IC DESIGN FLOW

4.1 Introduction

Due to the increasing levels of integration available in CMOS technology and the growing requirement for digital systems to communicate with the continuous-valued external world, there is an emerging need for establishing reliable and efficient design methodology to predict mixed-signal ICs performance [67], [68]. Standard-cell ASIC uses predesigned and certified logic cells, such as AND gate, and OR gate, from the foundry. The advantages of this approach are shorter design cycle and reduced risk. This section explores the details including both digital front-end and back-end designs. The established flow is used to implement high-speed ADC, high-speed DSPs, and related digital control blocks in Chapter 5 and Chapter 6.

4.2 Digital Front-End Design

Figure 4.1(a) captures the overview of ASIC flow. The digital design is partitioned into two stages: front-end and back-end. The front-end design deals with describing the operation of synchronous digital circuits in register transfer level (RTL). Usually, a circuit's behavior is described in terms of the data transfer between hardware registers and logical operations performed on those signals. The tool used for this section

is the Design Compiler from Synopsys. The input to the synthesis tool is a RTL hardware description, and the resulting output is a technology dependent gate-level netlist, as shown in Figure 4.1(b). On the other hand, the back-end design emphasizes on the physical layer designs of floorplanning, placement, and routing. After physical design, the post-layout netlist can be imported into Cadence Virtuoso Analog Design Environment (ADE) for mixed-signal verification.

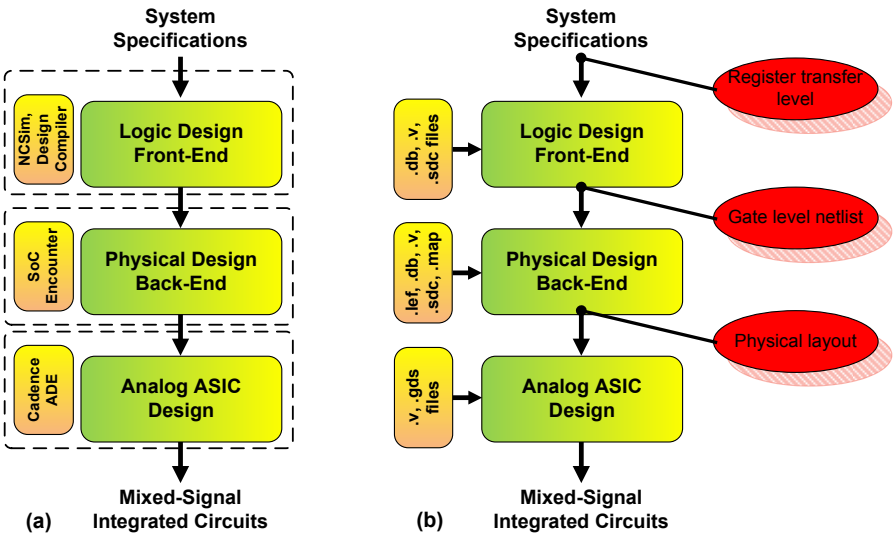

Figure 4.1: (a) High-level ASIC design flow; (b) I/O interfaces at different design stages.

4.2.1 Digital Front-End Design Flow

Figure 4.2 highlights the important steps in a digital front-end design. In the beginning, the functional description and the system specifications abstract important properties, such as performance model, to emulate the system using high-level language.

This stage can be clearly defined using state diagrams. Once the overall system architecture is derived, the detailed ASIC design can commence. This begins by developing and converting the high-level state diagrams into Verilog codes consisted of individual modules to ensure that the digital function specifications are correctly interpreted. In addition to capturing the design, a set of test cases in Verilog can be performed parallelly. The RTL Verilog should be synthesizable when automatic logic synthesis is used. Using the developed Verilog and testbenches, RTL verification based on the simulation engine of NCSim or ModelSim is performed thoroughly to validate the functionality against the specifications. In practice, it is common to spend 80 % of the design cycle writing and simulating Verilog at the register transfer level, and the remaining time is allocated to synthesizing and verifying the gates.

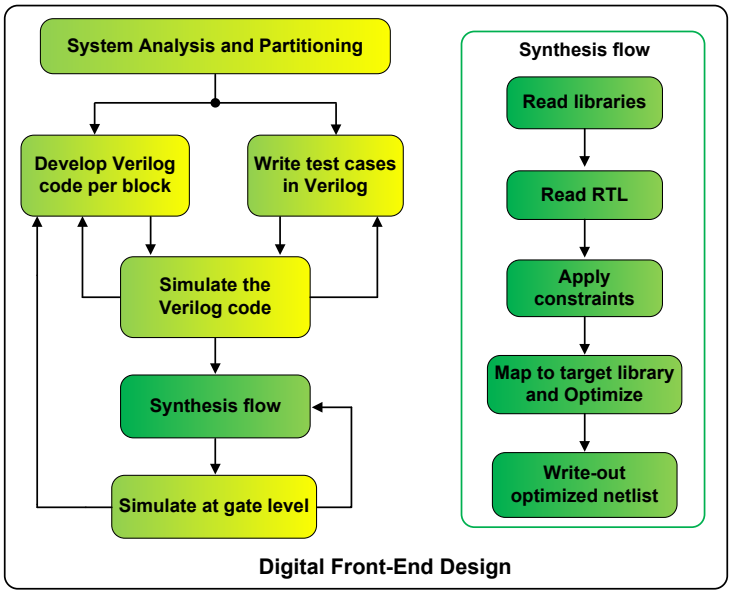

Figure 4.2: Digital front-end design flow.

4.2.2 Digital Synthesis Flow

The synthesis flow begins by converting a behavioral Verilog into a netlist using standard-cell library. Libraries using low threshold voltage cells can operate at higher speeds, but come with an associated higher leakage current. To estimate area and perform static timing analysis, timing models in design database (DB) format need to be provided. The DB files contain wireload models and timing/area information for each standard cell. As a result, the best, worst, and nominal process-voltage-temperature (PVT) corners can be easily analyzed to estimate positive or negative slack in the design. The design can also be elaborated to ensure that flip-flops are not being accidentally inferred. Moreover, the design consistency has to be checked against variations, such as unconnected ports, connection class violation, and hierarchy definitions. For high-speed sequential circuit, the input and output interfaces always consist of registers to guarantee certain timing. Therefore, a timing constraints file is required, and specifies the clock period, the arrival of certain input signals, the drive strength of input signals, and the capacitive load on output signals. This timing constraint file should be described in the Synopsys design constraints (SDC) format. For example, if the drive strength of an input signal is too weak, the tool chooses a smaller input logic so that the timing is not affected. To achieve gigahertz sampling speed, the tool optimizes the design based on logic restructuring and remapping cells. Before writing out the optimized netlist, setup violations should be fixed. On the other hand, hold time violations can be corrected in the physical design stage, as the extra parasitic delay due to interconnects and metal coupling could resolve this issue.

4.2.3 Static Timing Analysis

Static timing analysis is a method of computing the expected timing of a sequential data path without physically simulating it in ADE. In a synchronous digital system, data propagates and follows each tick of the clock signal using flip-flops. Figure 4.3(a) shows the data path, where the input and output are connected to a flip-flop. Notice that the arrival of clock signal to each flip-flop experiences different delays, denoted by T_{skw1} and T_{skew2}, respectively. To estimate maximum and minimum operating frequencies, a combinational block is inserted in the data path with a minimum delay of T_{min} and a maximum delay of T_{max}.

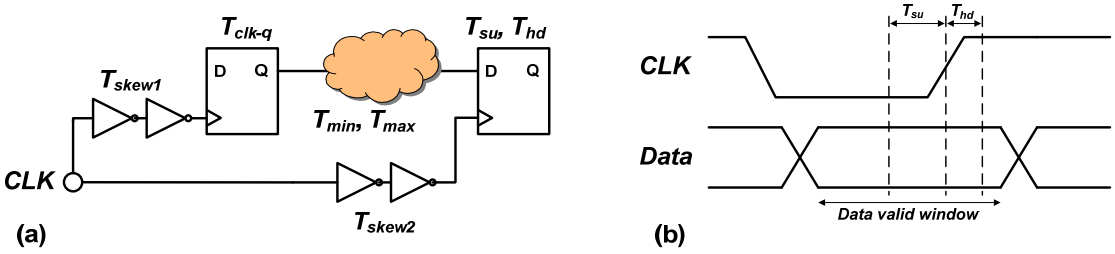

Figure 4.3: (a) High-speed data path; (b) Required setup time and hold time.

To first order, only two kinds of timing errors are considered in this system: setup time violation and hold time violation. Figure 4.3(b) illustrates the timing diagram for the required setup and hold time. Basically, setup time is the minimum time for which the data has to be stable before the clock edge arrives. Hold time requires data to be stable for

a short period after the clock edge arrives. To avoid setup time violation in Figure 4.3(a), the maximum clock period is derived:

$$T_{clk} + T_{skew2} > T_{clk-q} + T_{\max} + T_{su} + T_{skew1}, \tag{4.1}$$

where T_{clk} is the maximum clock period, T_{skew1} and T_{skew2} are the additional clock skews to the input and output flip-flops, respectively, $T_{clk\text{-}q}$ is the clock-to-Q delay of flip-flop, T_{su} is the setup time of flip-flop, and T_{max} is the maximum data path delay due to combinational block. For a high-speed digital system, the maximum operating frequency is highly associated with the chosen technology. The approximated $T_{clk\text{-}q}$ and T_{su} in 90 nm CMOS process are around 100 ps. Assuming zero skew and a combinational logic delay of 200 ps, the maximum clock period is roughly 400 ps, which corresponds to a maximum frequency of 2.5 GHz. If higher frequency is desired, then extra delay can be added to T_{skew2}. Another technique to meet STA is to target all the standard cells to a lower threshold voltage library. Unlike the setup time violation, the hold time violation happens when data passes through two consecutive flip-flops in a cycle. This is also known as the race condition. To avoid a race condition due to hold time violation, the following expression must be satisfied:

$$T_{hd} + T_{skew2} < T_{clk-q} + T_{\min} + T_{skew1}, \tag{4.2}$$

where T_{hd} is the maximum hold time for the flip-flop, and T_{min} is the minimum data path delay due to combinational block. The hold time can be met easily since the clock-to-Q delay of flip-flop is usually longer. In addition, the physical layout and interconnects add extra delay to the data path. An optimized gate-level netlist with a

minor hold time violation could be resolved in the physical design stage. However, hold failures are very difficult to correct after tape-out, and usually involve a very costly re-designing since hold violation cannot be corrected by reducing the clock frequency. On the contrary, setup failures can be solved by increasing clock period.

4.3 Digital Back-End Design

After importing the optimized gate-level netlist from the synthesis tool, the digital back-end design features an automatic place and route flow. The tool used for this section is the SoC Encounter from Cadence. Along with the synthesized netlist, additional timing libraries and physical libraries are required. For example, the standard cells need to be provided in library exchange format (LEF). A LEF file contains two important parameters to set up the database environment. First, technology information specifies routing layer, design rules, via definitions, and metal capacitance of standard cells. The design rules are stipulated by the foundry, and need to be strictly adhered to for reliable manufacturing. Second, the macros, such as cell descriptions, cell dimensions, and layout of pins and blockages, are required for highly compacted placement. In a digital back-end flow, as shown in Figure 4.4, four important stages are considered: floorplanning, placement, clock tree synthesis, and routing/optimization.

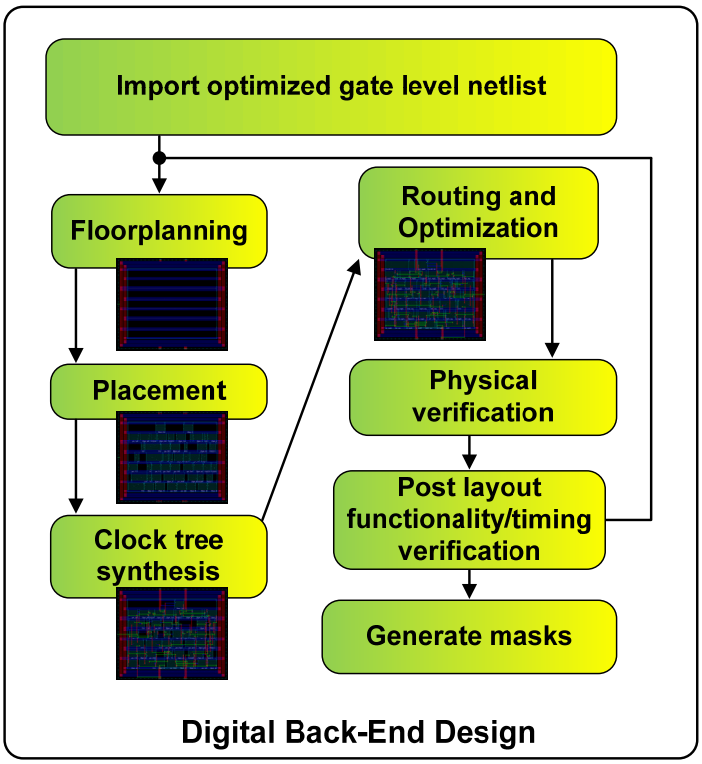

Figure 4.4: Digital back-end design flow.

4.3.1 Floorplanning

The first stage of digital back-end design flow is floorplanning. This stage takes a synthesized netlist which describes the design and the interconnection between different blocks to physical representation. The main objective of floorplanning is to minimize area and delay. During floorplanning, the core boundary is first decided by choosing an aspect ratio or an explicit chip dimension. Pin location and the metal layers for each pin are also specified here. Following I/O assignment, power planning creates a wide metal ring around the chip to ensure that the power/ground mesh is well distributed before the standard cells are placed. A wide metal ring is needed to reduce static IR drop due to

current flow in the metal interconnect lines. To further save area, the power mesh uses double back rows where every alternate cell row is flipped so that the *VDD* and *GND* for two consecutive rows of standard cells can be shared.

4.3.2 Placement

In this step, the standard cells location is defined to a particular position in a row. By running a timing driven placement, the tool ensures that the timing constraints specified in the SDC file are met at the placement stage. This is done by placing the cells based on their connectivity to the top level I/O pins. The main function of the placement algorithm is to make the chip as dense as possible, thereby minimizing the total wire length to reduce signal arrival time. In addition, the number of horizontal/vertical interconnects crossing a line should be minimized. Timing optimization is an option if the setup violation is not cleared after placement.

4.3.3 Clock Tree Synthesis

Clock tree synthesis is an important step for high-speed data paths. In large designs, the distribution of clock and high fanout nets should be considered before laying the regular routes. For example, clock signals are typically loaded with the greatest fanout and operate at the highest frequency among all signals. The timing or the arrival of clock signals becomes less predictable at high-speed high-fanout nodes. Therefore, the insertion of a highly-balanced clock tree distributes the clock signals from a common

point to all the elements that need it. This tool buffers the high-fanout nets to meet the loading requirements based on the number of gates that the clock port sees. However, if the clock skew is not within a tolerable time period, as shown in (4.1) and (4.2), it can cause disastrous hold time failures.

4.3.4 Routing and Optimization

In routing, various blocks in the chip are connected. Routing is split into two steps: global routing and detailed routing. Global routing uses a quick routing algorithm where the chip is divided into small blocks, and the congestion in each block is analyzed. Global routing assigns nets to specific gcells but it does not define the specific tracks for each of them, and the track assignment keeps track of how many interconnects are going in each direction without causing congestion. The actual connection between all the nets takes place in detailed routing. This step creates the actual via and metal connections with a main objective to minimize the total area, wire length, and delay in the critical paths. After detailed routing is complete, the exact length and the position of each interconnect in the design is known. The corresponding post-route delay can be written to the standard delay format (SDF) file, which describes the gate delay as well as the interconnect delay. After routing, STA is performed again to ensure that all setup and hold time failures do not exist at this stage. Timing violations that are not resolved by the physical tool need to be modified manually. For example, whenever there is additional logic to be added, engineering change order (ECO) operation is used to insert the logic directly into the netlist without changing other routes. Using the generated standard parasitic exchange

format (SPEF) file, an extracted simulation can be launched to determine the maximum speed of operation. The SPEF file includes the parasitic information, such as resistance, capacitance, and inductance of wires. After extraction verification is complete, filler cells are added to fill the gaps between standard cells. This final step removes possible design rule check (DRC) errors caused by N-well discontinuity in the layout.

4.4 Summary

This chapter describes the critical ASIC design flow developed in this thesis to realize high-speed digital ICs for multi-gigabit mixed-signal demodulator systems. Standard-cell ASIC is chosen by exploiting the accuracy and the reduced time offered by the synthesis and physical tools. This approach minimizes the risk and maximizes the design reliability. The fundamental limit in high-speed digital ICs is demonstrated in (4.1) and (4.2), where the setup time violation should be minimized by choosing the appropriate flip-flop topology, using a more advanced CMOS technology, or reducing the chip area. Those are the most direct parameters to improve the maximum clock frequency of synchronous digital systems.

CHAPTER 5

LOW-POWER COHERENT BPSK DEMODULATOR

5.1 Introduction

The rapid development of modern communication systems, such as the 60 GHz wireless devices with ultra-high data rates, drives the demand of data converters with ever-increasing sampling rates [69], [70], [71]. In order to simultaneously meet the ultra-low power requirement for portable electronic devices and the extremely-high sampling rate, it is absolutely necessary to simplify the architecture of ADCs as much as possible by excluding all non-essential blocks that increase power consumption and limit the sampling speed. This chapter first discusses a low-power 3-bit flash ADC design followed by detailed measurement results. Using the implemented ADC, a novel mixed-signal coherent BPSK demodulator based on Costas loop theory is developed, characterized, and measured. This coherent demodulator demonstrates low energy efficiency and multi-gigabit data transmission, which is suitable for millimeter-wave low-power radios. Detailed system and circuit implementations are also discussed.

5.2 Low-Power 3-bit Flash A/D Converter

Among all types of ADCs mentioned in Chapter 3, flash converter is the most suitable architecture based on the performance requirement for 60 GHz wireless

applications. The minimum latency guaranteed by the flash architecture is especially critical for mixed-signal single-carrier phase recovery systems (to be shown in Section 5.3). The performance of ADCs can be improved by means of either analog or digital calibrations. Calibration techniques improve the overall performance at the expense of increased circuit complexity, but often degrade the inter-stage bandwidth, linearity, and gain due to the presence of switches or series-input capacitor [50]. One offline calibration scheme proposed in [72] requires more than twice the area occupied by the ADC core. In a highly-integrated wireless radio for mobile applications, both the power consumption and area available for data converters are extremely limited.

5.2.1 ADC Architecture

Typically in the design of ADC, T/H circuit is the first component that provides instantaneous sampling of the input signal and holds its output at the sampled level for the rest of the clock period. Charge redistribution from the nonlinear parasitic capacitance and the sampling capacitor indicate distortion while this output slowly settles to its final state. In order to avoid this distortion, T/H circuit must provide high bandwidth, which requires higher power consumption. In this chapter, extremely low power consumption is targeted; hence in the first proposed ADC design, T/H circuit is excluded. Consequently, the design of high-speed comparator becomes critical and requires optimization.

By placing N converters in parallel and interleaving them, the clock frequency for each converter can be reduced while maintaining the same system throughput [73], [74],

[75], [76], [77]. Figure 5.1(a) shows an ADC architecture operating in two-channel (N = 2) time-interleaved manner, and its related timing diagram is shown in Figure 5.1(b). The first channel, ADC_A, samples the input at the falling edge of clock, while the second channel, ADC_B, samples at rising edge. The output multiplexer combines the data using *CLK* to produce a binary data stream, *Z*, at twice the data rate.

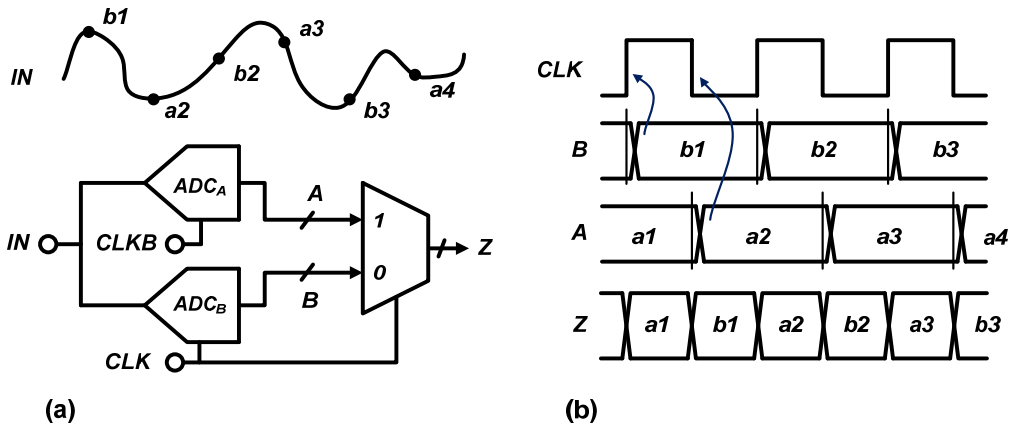

Figure 5.1: (a) Time-interleaved architecture; (b) Two-channel time-interleaved timing diagram.

In a system where large number of interleaved channels is adopted, the gain and offset mismatch between the channels limits the accuracy of ADCs unless trimming or calibration techniques are utilized. The inter-channel offset mismatch and offset mismatch give rise to fixed distortion and appears at

$$\frac{f_s}{N} \cdot n, \tag{5.1}$$

where f_s is the sampling frequency, N is the number of channels, and n = 0, 1, ..., N-1. This distortion is not signal dependent. Unlike the offset mismatch, the gain mismatch creates spurious tones at the output due to the multiplication of the input signal with periodic impulse train. This distortion noise can be found at

$$\frac{f_s}{N} \cdot n \pm f_{in}, \tag{5.2}$$

where f_{in} is the input frequency, and n = 1, 2, ..., N-1. All the tones appear at frequencies corresponding to the input signal. The use of multiple channels achieves higher sampling rate, but comes with associated distortion penalty. Figure 5.2 consists of 2^N-1 taps of reference voltages, high-speed latched comparators, CMOS buffers, and a high-speed digital encoder. Unlike the conventional flash architecture, this design removes T/H circuit and preamplifier to enable ultra-low-power processing and uses only two-channel interleaved architecture [47], [53].

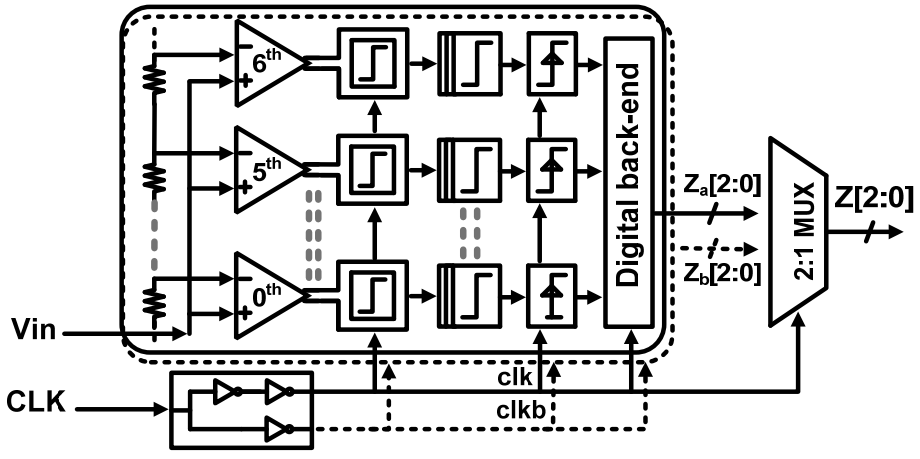

Figure 5.2: Block diagram of the 3-bit flash A/D converter.

5.2.2 High-Speed Optimizations

5.2.2.1 Comparator Optimization

Two practical issues in high-speed comparator design are: technology dependent gain bandwidth (GBW) product constant of an amplifier and the poor isolation between the latch output and the input of the preamplifier through the drain-gate capacitances of input transistors, inducing strong kick-back noise to the preceding stages. Unlike the switched-cascode comparator in [77], Figure 5.3 shows the current-mode latched comparator for the low-power ADC operation that can solve these two problems.

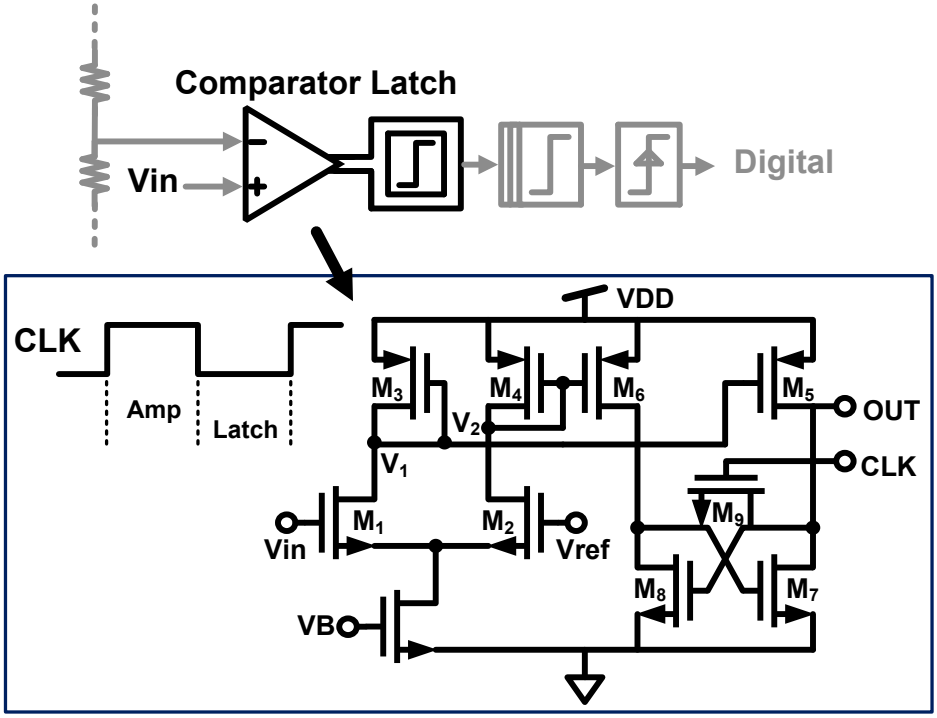

Figure 5.3: Schematic of the high-speed comparator.

First, the bandwidth requirement for high-speed operation during comparator amplification phase is defined as

$$BW_{INTER} > (n+1)\cdot \ln(2)\cdot f_s / 2\pi \,, \tag{5.3}$$

where n is the number of resolution, and f_s is the sampling frequency. (5.3) assumes half of the sample period is used for settling [78]. With n = 3, the minimum bandwidth for settling is: BW > 0.88 $f_{Nyquist}$ for time interleaving operation. Secondly, the input differential pairs before the latch has the advantage of reducing the input offset voltage of the latch and the gain is also enhanced from the current mirroring. The overload recovery time is determined by M_9, the output parasitic capacitance and the transconductance of M_7-M_8. The comparator is optimized based on the trade-offs of gain and total input-referred thermal noise during the amplification phase (CLK = 1) without considering flicker noise, as shown below:

$$A_V \propto \frac{g_{m1}\dfrac{W_5}{W_3}R_{on,9}}{4-2g_{m7}R_{on,9}}, \tag{5.4}$$

and

$$\frac{\overline{V_{n,in}^2}}{\Delta f} \propto 16kT\left(\frac{\gamma}{g_{m1}}+\frac{g_{m3}\gamma}{g_{m1}^2}+\frac{g_{m5}\gamma}{g_{m1}^2(\dfrac{W_5}{W_3})^2}+\frac{2-g_{m7}R_{on,9}}{g_{m1}^2(\dfrac{W_5}{W_3})^2 R_{on,9}}\right), \tag{5.5}$$

where coefficient γ is a constant depending on the technology, k is the Boltzmann constant in Joule/K, and T is the absolute temperature in Kelvin. As seen from (5.4) and

(5.5), to minimize thermal noise and resolve higher resolution, the transconductance of $M_{1\text{-}2}$ and the width of $M_{5\text{-}6}$ must increase.

5.2.2.2 Data Path Optimization

In Figure 5.4, the output of the comparator interfaces with a buffer consisting of two inverters. The trip point of the first inverter is resized low to avoid unnecessary switching power during the amplification phase when *CLK* is high.

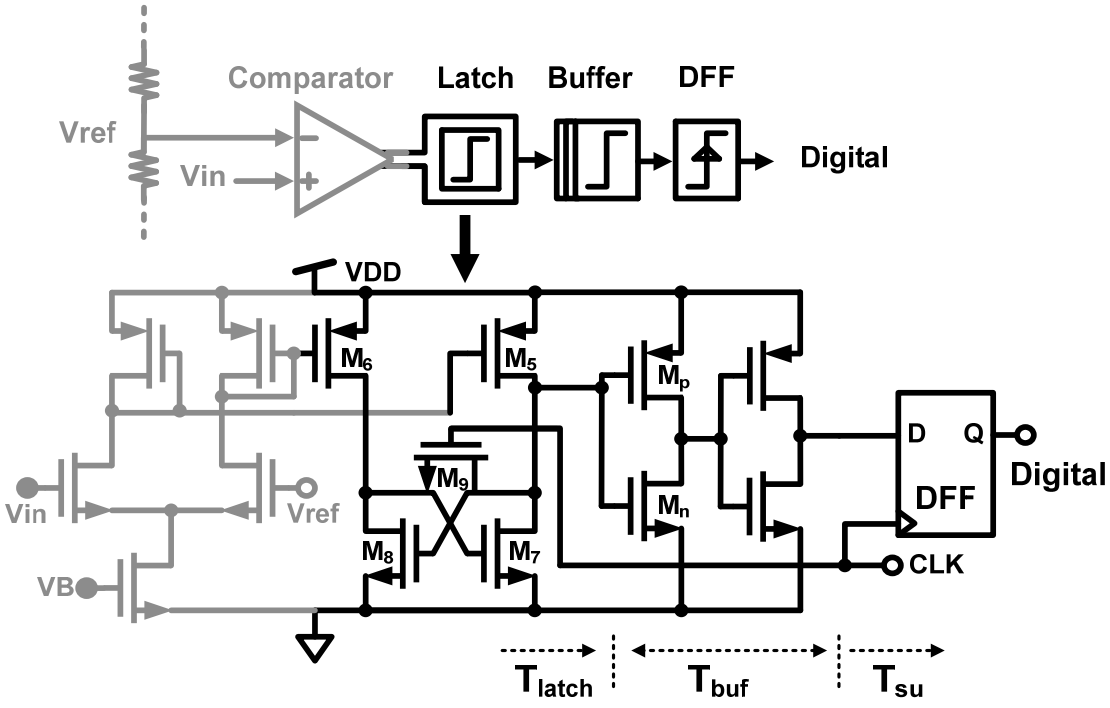

Figure 5.4: Schematic of the high-speed data path.

The timing constraint for the highest achievable speed is governed by the setup time (T_{su}) of the D flip-flop (DFF). Since the propagation delays due to comparator (T_{latch}) and buffer (T_{buf}) constitute enough margin for hold time, the only possible error is caused by the inadequate margin of setup time. The maximum clock frequency is derived:

$$\frac{1}{T_{CLK}} \leq \frac{1}{2 \cdot (T_{LATCH} + T_{BUF} + T_{SU})}. \tag{5.6}$$

Figure 5.5 shows the timing diagram of the interface between high-speed latched comparator output and digital data path. From the simulation, the worst case delay from each path is: T_{latch} = 90 ps, T_{buf} = 20 ps, and T_{su} = 75 ps, which corresponds to a maximum conversion rate of 2.7 GHz.

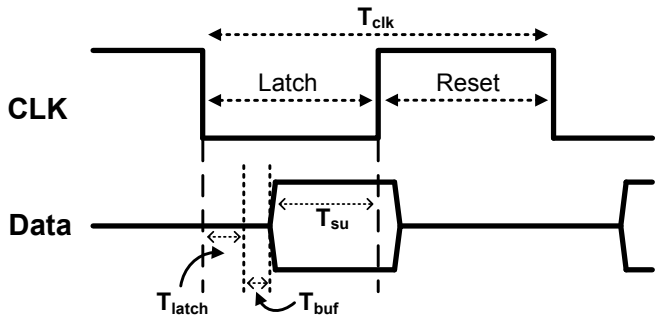

Figure 5.5: Critical timing diagram of the high-speed data path.

5.2.3 Measurement Results

The proposed ADC chip occupies an active area of 90 µm x 120 µm. It is fabricated in a 90 nm single-poly seven-metal (1P7M) CMOS process. The

microphotograph and test setup are shown in Figure 5.6. This measurement setup is able to perform both static and dynamic characterization. The static measurement is done by applying step voltages to the ADC input and its output data acquisition is performed using a ByteParadigm FPGA board. To measure dynamic performance, a high-speed ADC-DAC test is performed and its output spectrum is captured using a spectrum analyzer from Rohde & Schwarz FSU 1166. A 1.8 V power supply is only used for the output 50 Ω buffer to facilitate spectrum analyzer measurement. Otherwise, the ADC core only consumes 1 V power supply.

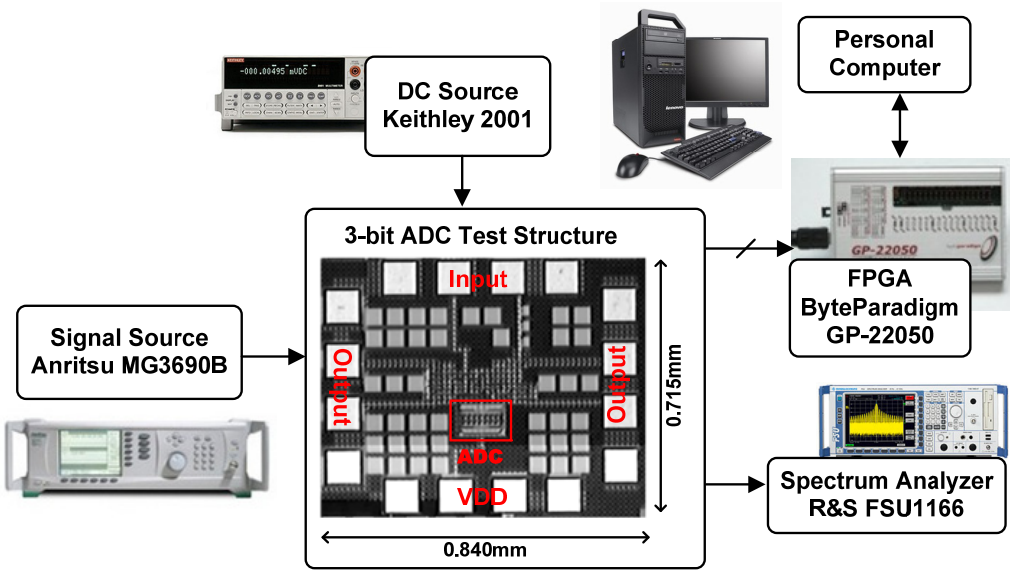

Figure 5.6: Measurement setup and microphotograph of the ADC test chip.

The measured static performance of the ADC is shown in Figure 5.7. At 3 GS/s operating, the peak DNL and integral nonlinearity (INL) are both 0.4 LSB. Since the

absolute value of DNL and INL is less than 1 LSB, and 0.5 LSB, respectively, no missing code is observed, and thereby monotonicity is guaranteed. Figure 5.8(a) captures the output spectrum with a 346 MHz input at 3 GS/s. The same output is further observed at 5 GS/s when input frequency is increased to 834 MHz, as shown in Figure 5.8(b). From both spectrum plots, the error due to the INL is also estimated to be less than 1 LSB since the fundamental tone is at least 6*n* dB (in our case 18 dB) above all the individual harmonics and distortions, where *n* is the theoretical number of bits [79].

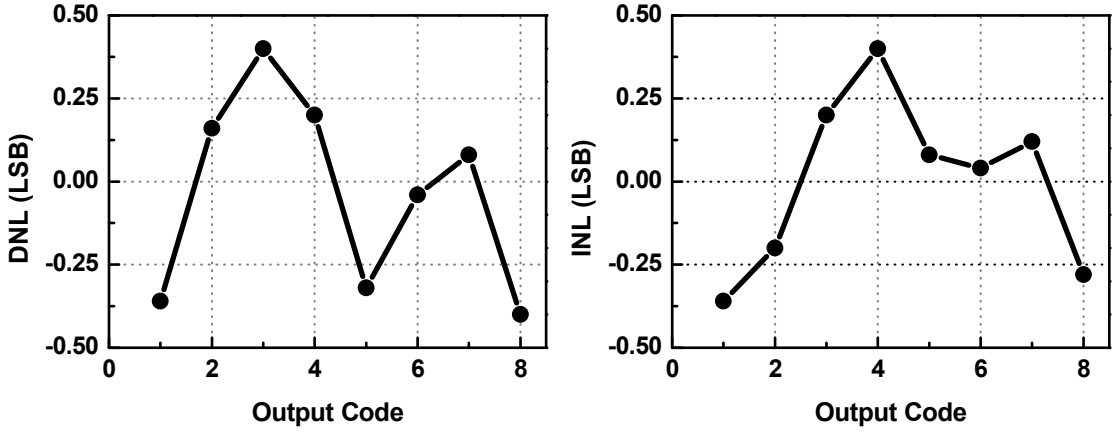

Figure 5.7: Measured DNL/INL at 3 GS/s.

The dynamic performance is characterized in Figure 5.9(a) and Figure 5.9(b). This ADC achieves spurious free dynamic range (SFDR) of 23.2 dB at 3 GS/s and 19.84 dB at 5 GS/s with 346 MHz and 834 MHz input, respectively. With the same input frequencies, its measured SNDR are 16 dB at 3 GS/s and 14.73 dB at 5 GS/s. The SNDR curve in Figure 5.9(b) indicates an effective resolution bandwidth (ERBW) of 1.25 GHz

at 3 GS/s and 1.15 GHz at 5 GS/s, respectively. At 3 GS/s operation, the measured SNDR is above 15 dB for input frequencies up to 1000 MHz and the SFDR is above 20 dB for input frequencies up to 850 MHz. Its ENOB is 2.37 up to a conversion rate of 3 GHz.

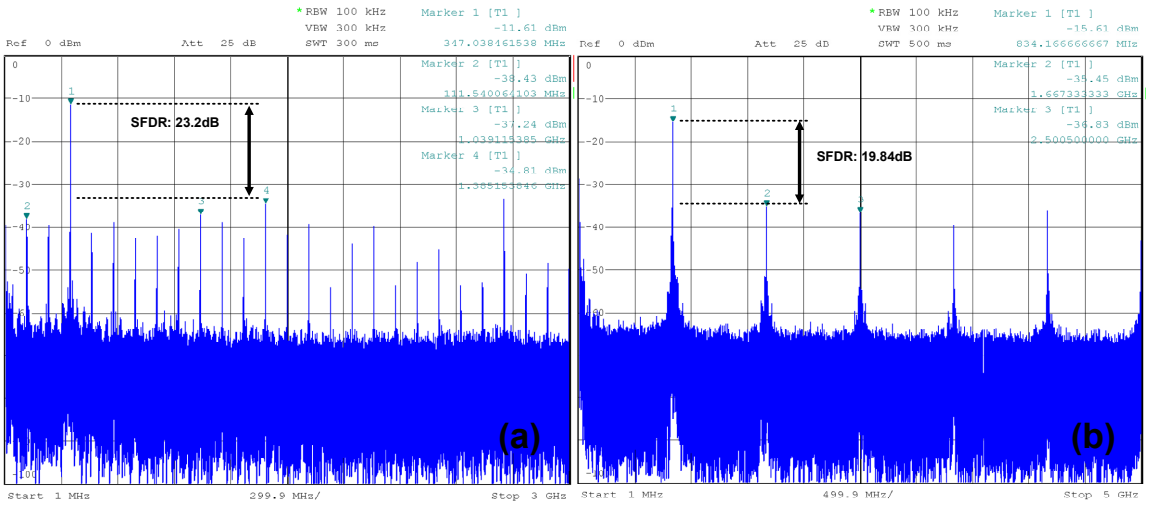

Figure 5.8: (a) Measured spectrum of 346 MHz input at 3 GS/s; (b) Measured spectrum of 834 MHz input at 5 GS/s.

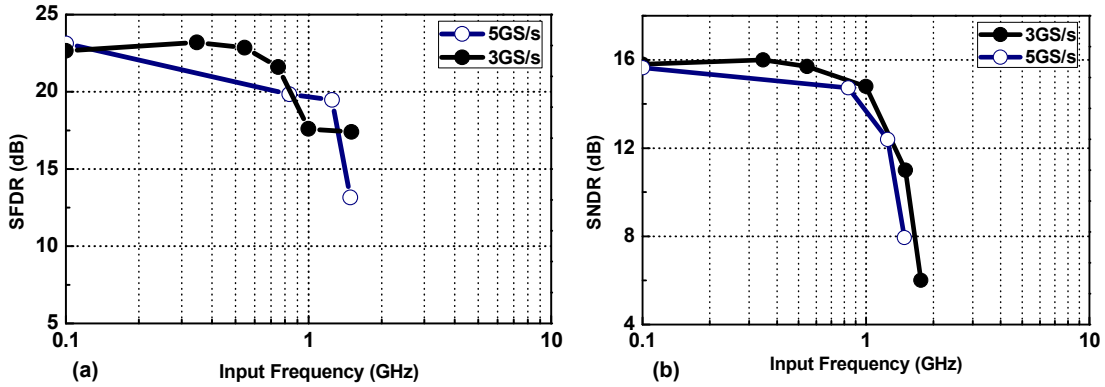

Figure 5.9: Measured (a) SFDR and (b) SNDR versus input frequencies.

A two-channel time-interleaved high-speed 3-bit flash ADC in 90 nm CMOS is presented in this section. In order to achieve excellent power efficiency, T/H circuit and preamplifier designs are removed, and only the very essential blocks are retained. Thorough optimizations are analyzed, and the results demonstrate an ultra-low-power (3 mW, 3.9 mW) and high-speed (3 GS/s, 5 GS/s) performance. The detailed performance of the measured ADC is shown in Table 5.1 and compared with the current state-of-the-art ADCs in Table 5.2, indicating one of the most power-efficient high-speed converters and the best power efficiency for an ADC operating at both 3 GS/s and 5 GS/s. Degradations of the actual ADC performance include but are not limited to power and ground bounce, comparator random offset mismatch, INL/DNL of the DAC used in the direct ADC-DAC testing, 50 Ω output buffer nonlinearities, signal source distortion, and output harmonic distortions with no filtering. The measured ADC presents an opportunity for a multi-gigabit real-time digital processing at low power budget.

Table 5.1: Performance summary of the 3-bit flash ADC.

Specification	Parameter		Unit
Supply voltage	1		V
Input range	200		mVpp
Sampling rate	3	5	GS/s
Power consumption	3	3.9	mW
SFDR	23.2 @ fin = 346 MHz	19.84 @ fin = 834 MHz	dB
SNDR	16.0 @ fin = 346 MHz	14.74 @ fin = 834 MHz	dB
ENOB	2.37 @ fin = 346 MHz	2.15 @ fin = 834 MHz	bit
ERBW	1.25	1.15	GHz
FOM	0.35	0.465	pJ
DNL/INL	< 0.4		LSB
Active area	0.0108		mm^2

Table 5.2: Comparison with state-of-the-art ADCs.

Specification	[47]	[72]	[80]	This work		Unit
Resolution	4	4	4	3		Bit
Supply voltage	1.2	1.8	1.8	1		V
Sampling rate	1.25	1	4	3	5	GS/s
Power	2.5	10.6	43	3	3.9	mW
Area	0.033	0.021	0.06	0.0128		mm^2
Technology	90	180	180	90		nm
FOM	0.16	0.81	2.14	0.35	0.465	pJ

5.3 Coherent BPSK Demodulator

Recent publications have demonstrated CMOS wireless communication transceivers in the millimeter-wave regime, which offers several gigahertz of bandwidth [69], [70], [71]. Such systems generally require a low-power broadband demodulator in either analog, mixed-signal or digital domain, as shown in Figure 5.10. The analog approach limits the overview system complexity, but could be achieved with the lowest power consumption. The mixed-signal approach is the most desired method to achieve robustness and resolve complex modulation schemes simultaneously. On the other hand, the digital approach requires the use of extremely high sampling and medium-to-high resolution ADCs, resulting the worst receiver sensitivity. Therefore, the remaining chapter focuses on the broadband mixed-signal demodulator architecture and its related circuit implementation.

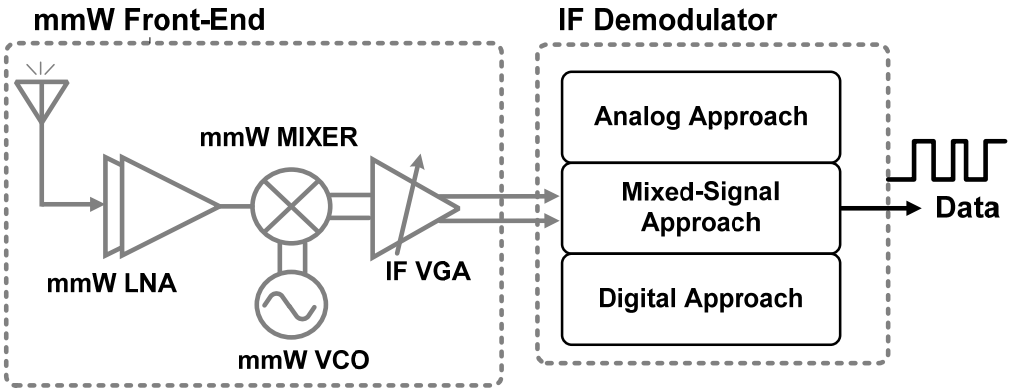

Figure 5.10: Example of a heterodyne receiver using millimeter-wave frequency bands.

5.3.1 Theory of Operation

One attractive method of obtaining a practical synchronous demodulator system is the concept of a Costas loop, as shown in Figure 5.11 [81], [82], [83]. This architecture detects a double-sideband suppressed-carrier (DSBSC) signal, such as BPSK, and involves two parallel tracking loops operating simultaneously from the same QVCO. Using an in-phase (I) coherent detector and a quadrature-phase (Q) coherent detector, an error signal, *e(t)*, can be calculated and applied to the QVCO to adjust the frequency and phase simultaneously. By means of negative feedback, a locking condition can be maintained when the local oscillator signal is exactly synchronized in both frequency and phase with respect to the modulated input signal.

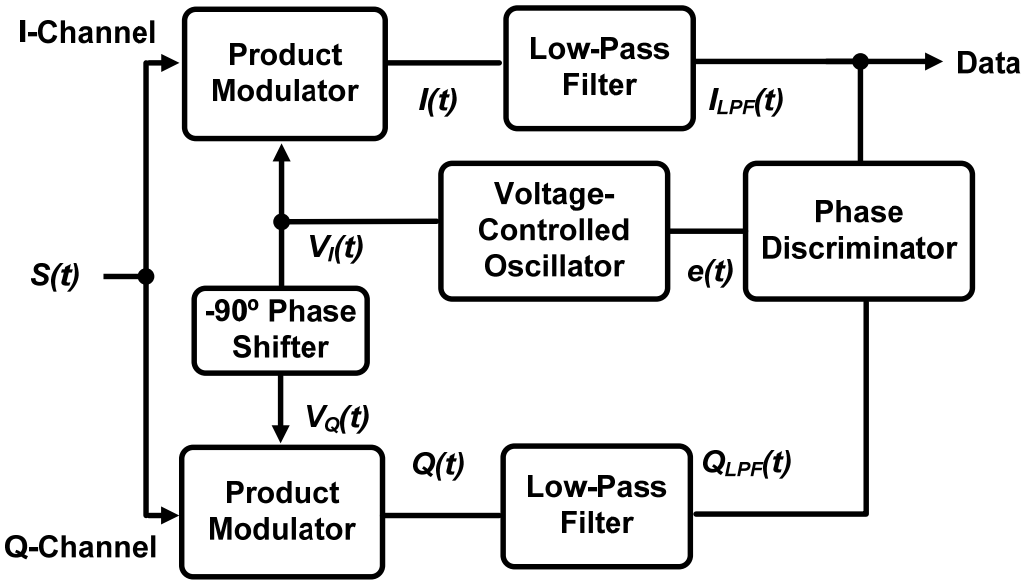

Figure 5.11: Functional diagram of Costas loop demodulator.

Consider the quadrature demodulator with a DSBSC signal of the form:

$$s(t) = data \cdot \cos(\omega_c \cdot t), \tag{5.7}$$

where *data* is a binary modulation of a ±1 digital waveform, and ω_c is the radian carrier frequency. The product modulator multiplies the DSBSC input signal with quadrature LO sources and generates down-converted signals in I channel and Q channel, respectively. Using trigonometric identities, the down-converted baseband signals become:

$$I(t) = \frac{1}{2} data \cdot [\cos((\omega_c + \omega_{vco}) \cdot t + \phi) + \cos((\omega_c - \omega_{vco}) \cdot t - \phi)], \tag{5.8}$$

and

$$Q(t) = \frac{1}{2} data \cdot [\sin((\omega_c + \omega_{vco}) \cdot t + \phi) - \sin((\omega_c - \omega_{vco}) \cdot t - \phi)], \qquad (5.9)$$

where ω_{vco} is the output radian frequency of QVCO with a constant phase error of ϕ relative to the input modulated carrier. After low-pass filtering, the signals to the phase discriminator become:

$$I_{LPF}(t) = \frac{1}{2} data \cdot [\cos((\omega_c - \omega_{vco}) \cdot t - \phi)], \qquad (5.10)$$

and

$$Q_{LPF}(t) = \frac{1}{2} data \cdot [-\sin((\omega_c - \omega_{vco}) \cdot t - \phi)]. \qquad (5.11)$$

Finally, the error signal is derived by multiplying $I_{LPF}(t)$ and $Q_{LPF}(t)$:

$$e(t) = \frac{1}{4} data^2 \cdot [-\sin(2(\omega_c - \omega_{vco}) \cdot t - 2\phi)]. \qquad (5.12)$$

By applying $e(t)$ back to the QVCO, phase and frequency synchronization is achieved. The Costas loop is analyzed by assuming the output frequency of the QVCO is locked to the input suppressed carrier frequency. When ω_c is equal to ω_{vco}, (5.10), (5.11), and (5.12) become a function of only the phase error term. Since the phase error near lock is very small, the resulting $I_{LPF}(t)$ should be at its maximum compared to that of $Q_{LPF}(t)$ (i.e., $\cos(\phi) >> \sin(\phi)$). This is the desired condition where the phase locking condition is maintained. The I channel then carries the demodulated data stream, while the Q channel produces a DC term, known as the quadrature null effect.

When there is sufficient SNR, the in-phase loop is often designed with a low-pass filter followed by a limiter, known as the hard-limiting Costas loop (refer to Figure 5.12). At high SNR, the limiter output has a sign during each bit interval that is identical to the present data bit polarity. The effect of hard-limiting speeds up the locking by the optimum estimate of the polarity [84]. The hard limiter implements a "sgn" function. Assuming the output frequency of QVCO is equal to the input suppressed carrier frequency, the limiter output can then be expressed as

$$\begin{aligned} I'_{LPF}(t) &= \mathrm{sgn}(I_{LPF}(t)) = \mathrm{sgn}(data) \quad for\ 0 \le |\phi| \le \pi/2 \\ &= -\mathrm{sgn}(data) \quad for\ \pi/2 \le |\phi| \le 3\pi/2 \end{aligned} . \tag{5.13}$$

Finally, the new error signal, *e'(t)*, due to hard-limiter becomes:

$$\begin{aligned} e'(t) &= \frac{1}{2}\sin(\phi) \quad for\ 0 \le |\phi| \le \pi/2 \\ &= \frac{-1}{2}\sin(\phi) \quad for\ \pi/2 \le |\phi| \le 3\pi/2 \end{aligned} . \tag{5.14}$$

The overall phase-error output of the hard-limited Costas loop has a larger linear range (wider pull-in range) than using the conventional analog multiplier Costas loop. Figure 5.13 compares the error signals response between the standard Costa loop and the hard-limited loop. The standard Costas loop covers a linear range from –π/4 to +π/4, whereas the hard-limited Costas loop achieves a wider range from –π/2 to +π/2. By using a hard limiter, the requirement of the phase discriminator can be relaxed. Therefore, the demodulator architecture with hard-limiting is desired when there is sufficient SNR.

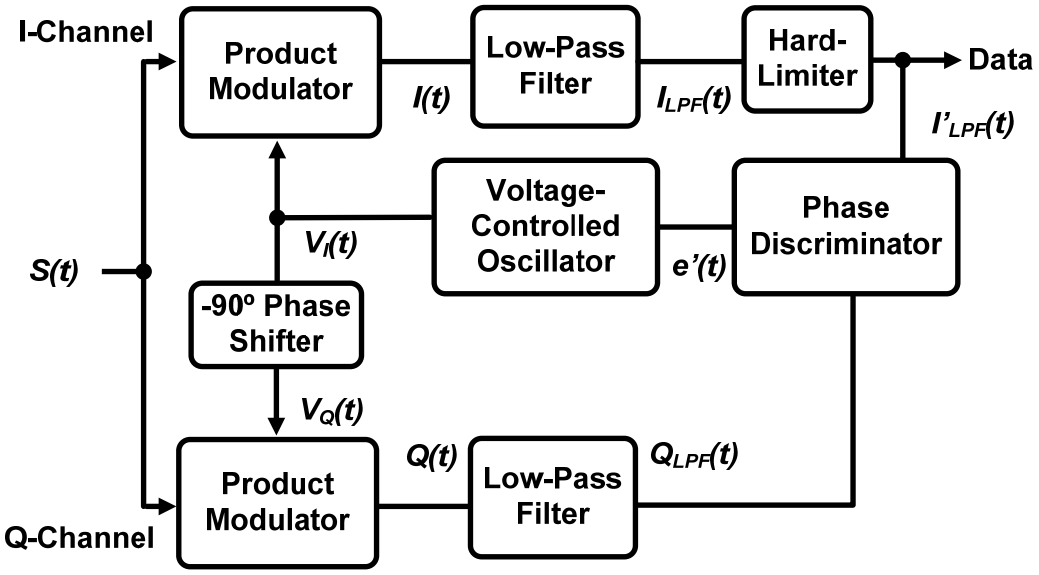

Figure 5.12: Functional diagram of Costas loop demodulator with hard-limited in-phase channel.

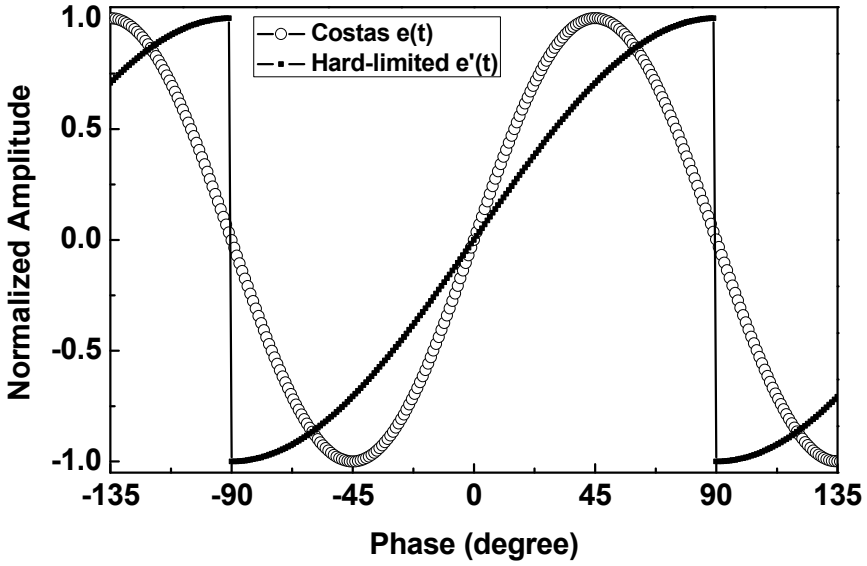

Figure 5.13: Error signals comparison.

5.3.2 Linear Model

The Costas loop essentially consists of two parallel phase-locked loops (PLL), where an error signal is generated in the control signal of the VCO. Unlike the error signal in (5.14), the analog multiplier is modified to an exclusive OR (XOR) operation, as shown in Figure 5.14. As a phase detector (PD), the analog multiplier and the XOR logic exhibit similar output characteristics. Considering the digital case in Figure 5.14(b), the XOR operation has an average output, $\overline{V_{out}}$, that is linearly proportional to the phase difference, $\Delta\phi$, between its two inputs, which is similar to the sine response from the conventional Costas loop.

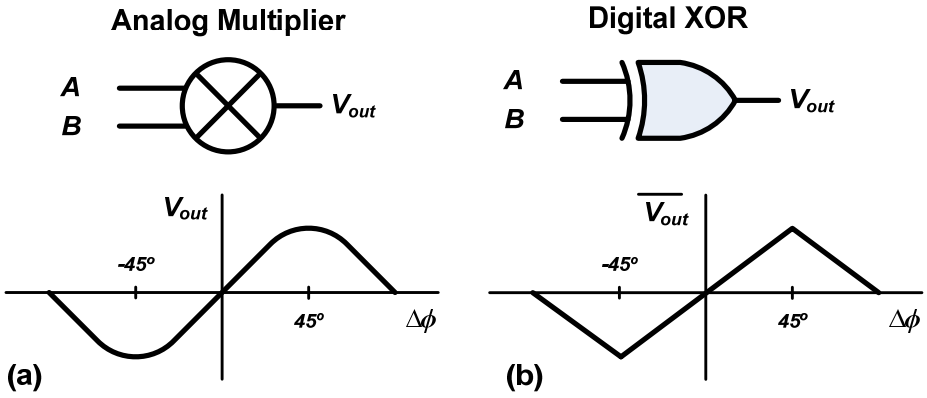

Figure 5.14: (a) Analog multiplier and (b) digital XOR gate as phase detector.

In the hard-limited Costas loop, the "sgn" function can be represented simply by the most significant bit (MSB) of ADC. This present data bit polarity is equivalent to its

input sign during each bit interval, and resembles the functionality of a hard-limiter. The sampled error signal (5.14) at any sampling instant, *t*, can be expressed as

$$e[t] = \text{sgn}(I_{LPF}[t]) \cdot Q_{LPF}[t] = \overline{(I[2^{N-1}-1],...,I[2^{N-1}-1]) \oplus (Q[2^{N-1}-1],...,Q[1])}, \qquad (5.15)$$

where *N* is the number of bits, *Q[1]* is the LSB in Q channel, $Q[2^{N-1}-1]$ is the MSB in Q channel, and $I[2^{N-1}-1]$ is the MSB in I channel. The expression in (5.15) actually implements an inverse of the exclusive OR (XNOR) operation due to the additional negative polarity of (5.11) resulting from Q channel down-conversion. Considering a 3-bit ADC, the multiplication of the in-phase loop and the quadrature-phase loop can be approximately modelled by $e[t] = \overline{(I[3], I[3], I[3]) \oplus (Q[3], Q[2], Q[1])}$ at any sampling instant. A higher number of bits resolves better accuracy with smaller quantization noise; hence the mapping from *sin(ϕ)* to binary representation is more accurate.

Figure 5.15 shows the linear model of the demodulator in *s* domain. To simplify the analysis, the linear model of the hard-limited Costas loop is assumed to be a third-order linear PLL using 3-bit XNOR as the phase detector.The PD tracks the input phase difference and converts its output to voltage domain using a high-speed DAC. The error amplifier (EA) isolates the DAC from the loop filter, followed by a level shifter and a low-pass filter. Here, the PD with a DAC output is modelled as

$$V_{pd\_dac}(\Delta\phi) = \frac{VDD}{4 \cdot \pi} \cdot \Delta\phi = K_{pd\_dac} \cdot \Delta\phi, \qquad (5.16)$$

where K_{pd_dac} is the phase detector gain normalized to the DAC output in volts per radian, and $\Delta\phi$ is the input phase tolerance from $-\pi/2$ to $+\pi/2$ for a hard-limited Costas loop.

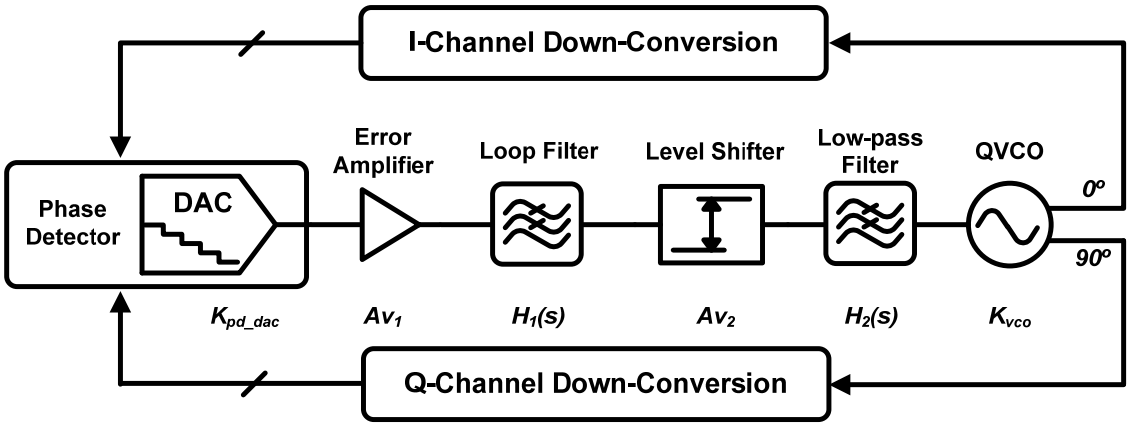

Figure 5.15: Linear model of the mixed-signal BPSK demodulator.

The loop filter, $H_1(s)$, consists of a pole and a zero, and is given by

$$H_1(s) = \frac{1 + \frac{s}{\omega_{z1}}}{1 + s \cdot (\frac{1}{\omega_{z1}} + \frac{1}{\omega_{p1}})}, \tag{5.17}$$

where ω_{z1} and ω_{p1} represent the pole and the zero in radians per second. An additional degree of freedom is gained by adding a zero in the TF. The level shifter then brings the DAC output voltage to roughly *VDD/2*, and drives another LPF to stabilize the locking voltage on the QVCO control line. The second filter TF is given by

$$H_2(s) = \frac{1}{1 + \frac{s}{\omega_{p2}}}, \tag{5.18}$$

where ω_{p2} is the second pole of the system. To guarantee stability, this pole frequency should be far away from ω_{p1}. The stability behavior of the Costas loop can also be analyzed graphically by deriving the open-loop TF:

$$H(s)|_{open} = \frac{\phi_{out}}{\phi_{in}}(s)|_{open} = K_{pd\_dac} \cdot A_{v1} \cdot H_1(s) \cdot A_{v2} \cdot H_2(s) \cdot K_{vco}$$

$$= \frac{K_{pd\_dac} \cdot A_{v1} \cdot A_{v2} \cdot K_{vco} \cdot (1 + \frac{s}{\omega_{z1}})}{s^3 \cdot (\frac{\omega_{z1} + \omega_{p1}}{\omega_{z1} \cdot \omega_{p1} \cdot \omega_{p2}}) + s^2 \cdot (\frac{\omega_{z1} + \omega_{p1}}{\omega_{z1} \cdot \omega_{p1}} + \frac{1}{\omega_{p2}}) + s}, \quad (5.19)$$

revealing one pole at origin. At $s=0$, the loop gain goes to infinity, indicating that the change in ϕ_{out} is exactly equal to the change in ϕ_{in}. As the frequency of the error signal increase, the tracking ability of the loop is weakened and attenuated with increasing phase error. As shown in Figure 5.16, the loop gain begins from infinity and falls at a rate of 20 dB/dec for input frequencies smaller than ω_{p1}, and at a rate of 40 dB/dec until the only zero, ω_{z1}, kicks in. The zero frequency is chosen between the two poles, ω_{p1} and ω_{p2}, to ensure a phase margin of 45 degrees or better up to 2 GHz. In this analysis, the exact zero and poles frequencies are 12.7 MHz, 2.54 MHz, and 1.59 GHz, respectively. The PD gain, the error amplifier, and the QVCO is chosen to be 0.25/π V/rad, 0.3 dB, and 3.5 GHz/V, respectively. Considering the loop settling time, the ripple on the control voltage, the phase error, and the stability of the Costas loop can be optimized based on the parameters of open-loop gain and passive values.

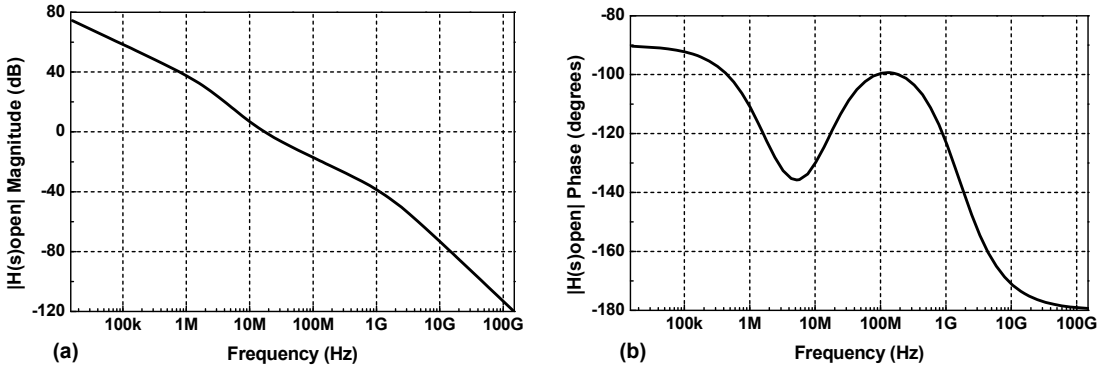

Figure 5.16: (a) Bode magnitude plot and (b) bode phase plot of the derived third-order system.

5.3.3 System Simulation

Since the Costas loop based BPSK demodulator relies on the feedback concepts related to PLL, simulation and verification in ADE will take considerable amount of time. Therefore, a system-level simulation is first performed in MATLAB Simulink to characterize the system behavior. In Figure 5.17, the BPSK modulator is created by converting a binary random data generator to bipolar (±1) format, followed by a loop-pass filter. The input data is then up-converted to 13 GHz IF frequency. Since the goal is to analyze the Costas loop, RF front-end parameters are not considered here. The demodulator on the receiver side involves three types of modeling: analog, mixed-signal, and digital. The analog portion consists of the models for product modulators, QVCO, amplifiers, loop filter TF, and error amplifier. The mixed-signal block involves the models for high-speed ADC and DAC. Finally, the digital block includes a high-speed pipelined phase discriminator.

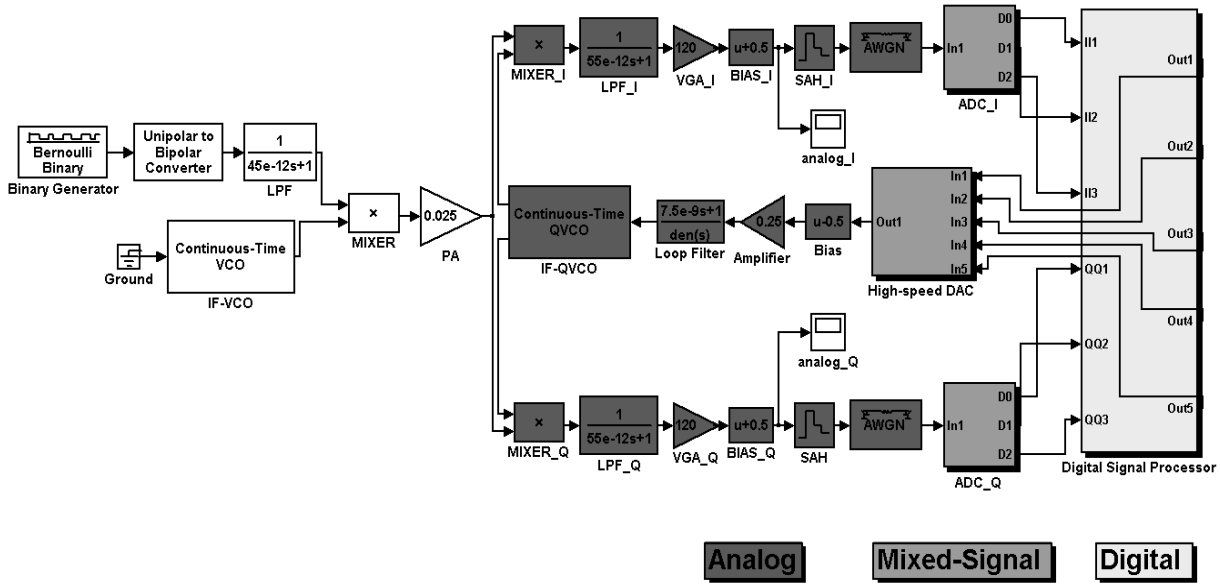

Figure 5.17: Simulation setup in MATLAB Simulink.

The simulated error signals using conventional Costa loop, hard-limited loop, and mixed-signal method are compared in Figure 5.18. The main disadvantages of mixed-signal approach are quantization noise, and extra loop delay caused by heavily pipelined digital circuits. Quantization noise can be suppressed by choosing the DAC in the feedback loop with a higher resolution than the sampling ADCs in the down-conversion paths. In this work, 5-bit DAC is chosen. The loop settling time is also a common disadvantage for any closed-loop systems.

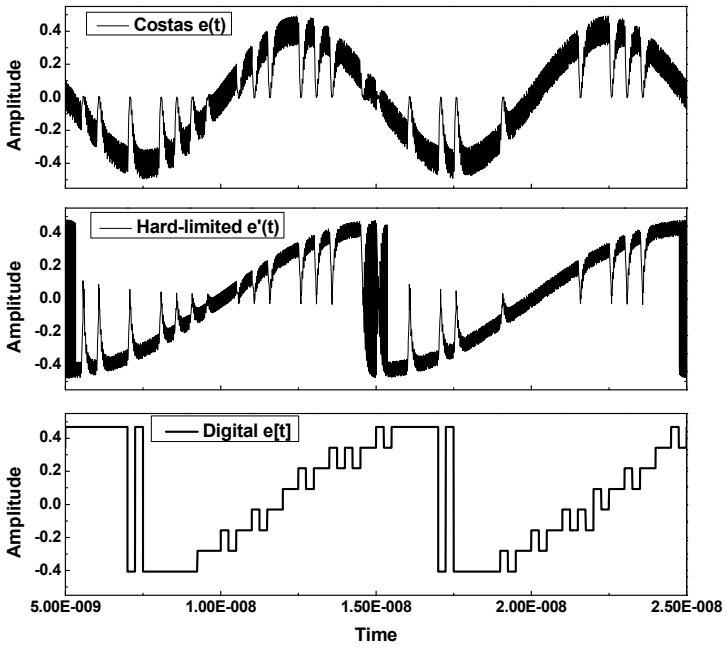

Figure 5.18: Simulated error signals using conventional, hard-limited, and mixed-signal approaches.

Figure 5.19(a) shows the BER simulation versus ADC resolution using mixed-signal synchronization architecture. The BER degradation due to the quantization noise and the nonlinearity of 3-bit and 4-bit ADCs are similar and can be negligible. As discussed in Chapter 3, the ADC trade-off between power and speed conveys 3-bit architecture over any higher resolution systems. Figure 5.19(b) further plots the demodulator synchronization range as a function of loop delays at various ADC resolutions. A data rate of 2 Gbps is chosen at an IF carrier frequency of 13 GHz. Since the demodulator is a feedback system and takes time to lock, the synchronization range is defined by whether the loop locks within the first 500 ns. As expected, when the loop delay is large, the inherent closed-loop system becomes unstable due to reduced phase

margin. The drastic reduction of synchronization range is a consequence of having excessive loop delay. At 3.25 ns, the synchronization range drops to 1 MHz, 10 MHz, and 40 MHz for 2-bit, 3-bit, and 4-bit resolution, respectively. Beyond, 3.25 ns, the carrier recovery loop fails to demodulate.

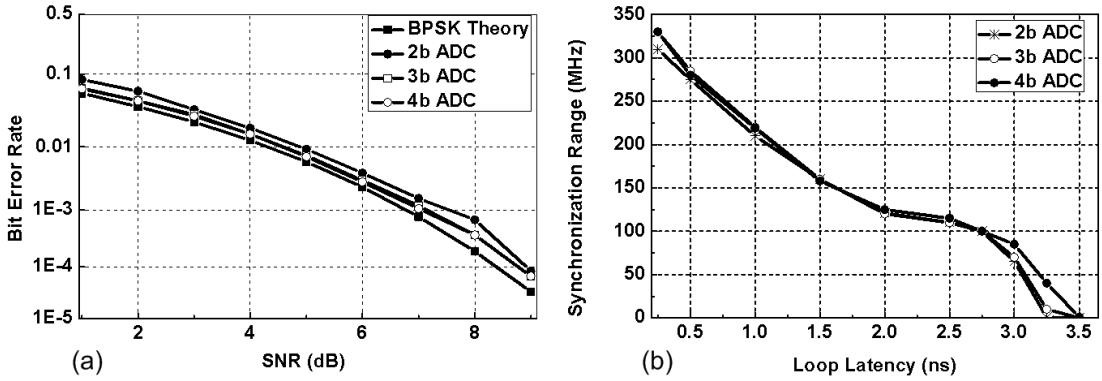

Figure 5.19: (a) BER simulation versus ADC resolution; (b) Synchronization range versus loop latency.

The simulation results also indicate that synchronization range increases directly with K_{VCO} gain. For example, the synchronization range increases by 40 % when the K_{VCO} gain is doubled. However, higher K_{VCO} results in poor phase noise performance. On the other hand, the synchronization range can drop 25 % for I/Q imbalance up to ±3 dB and DC mismatch up to 40 mV, respectively. The following three design considerations are concluded from the system-level simulation:

- 3-bit flash ADC architecture is chosen for its low latency and high speed.

- AGC loop is required to reduce I/Q imbalance.
- DC offset compensation is needed to minimize DC mismatch.

5.3.4 Demodulator Architecture

Figure 5.20 shows the simplified block diagram of the low-power mixed-signal demodulator that is primarily composed of analog front-end and mixed-signal back-end. The analog front-end consists of two passive mixers, 13 GHz QVCO, variable-gain amplifiers (VGA) with AGC loop and DC offset compensation. The high-speed mixed-signal integrated circuits consist of two 3-bit ADCs, a 5-bit DAC, and a high-speed DSP. The DSP tracks the phase difference between two channels to produce a lead/lag difference to correct the frequency offset between BPSK modulated input and QVCO outputs. The generated error signal is converted back to analog domain using a high-speed DAC, followed by an EA and low-pass filter, and eventually controls the tuning voltage of QVCO. Hence, the phase-locking of the QVCO outputs to the input signal is maintained. The described building blocks feature a high-speed demodulator architecture and can be realized using low-cost CMOS technologies.

Based on Costas loop theory, the advantages of the proposed mixed-signal demodulator are summarized:

- The mixed-signal BPSK demodulator offers an inherent ability to self-correct both frequency and phase offsets.

- The error signal, *e'(t)*, provides a wider linear range of ϕ.
- The simplicity of structure is suitable for multi-gigabit operation.
- The implementation is extremely low cost and low power.
- Since the carrier-recovery system requires embedded ADCs, higher-order modulation schemes are compatible using the same quadrature down-converter.
- The use of integrated ADCs enables digital signal conditionings, such as time-domain equalizer (TDE).

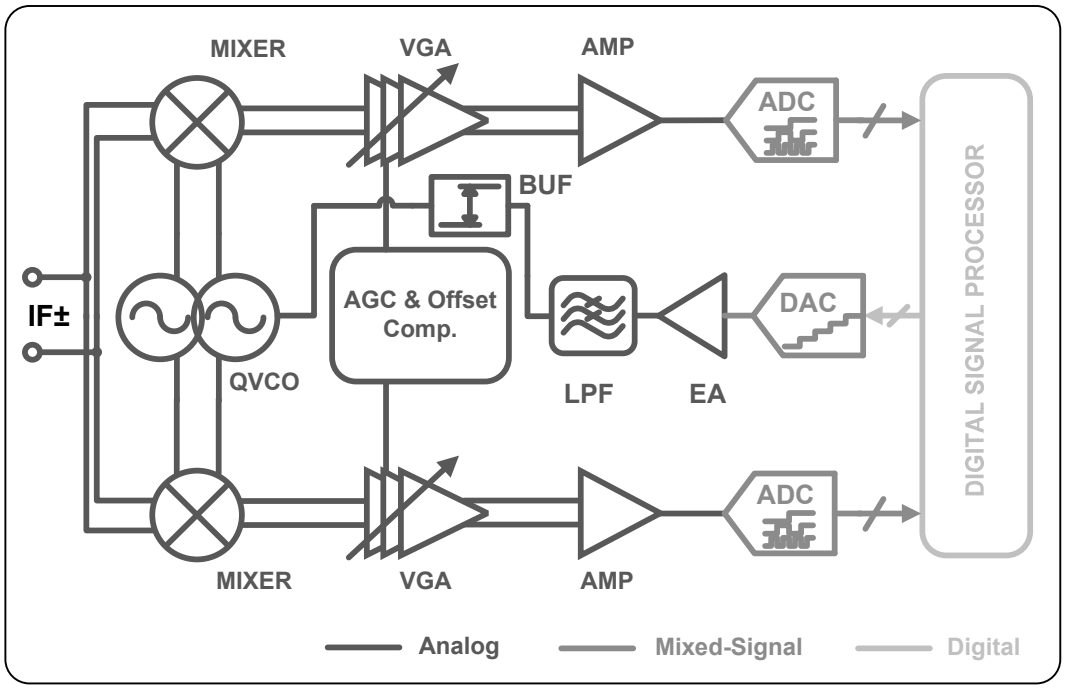

Figure 5.20: Block diagram of the multi-gigabit mixed-signal demodulator.

5.3.5 Circuit Implementation

5.3.5.1 Quadrature Controlled-Voltage Oscillator

Local oscillators are used in every transmitter, receiver, and transceiver system. Variable frequency enables a PLL system or a Costas loop based demodulator to correct frequency errors from the received signal or reference. Low phase noise ensures little interference with nearby channels, and its purity allows for higher-order modulation schemes, but requires high-Q resonator. High-Q resonator also provides a larger LO voltage swing to drive the mixer with greater linearity to allow higher conversion gain.

The QVCO is formed by coupling the two identical LC-tank oscillators to each other, as shown in Figure 5.21 [85], [86], [87]. The LC oscillator consists of a cross-coupled pair (M_1-M_2 and M_3-M_4) with a parallel LC tank formed by two varactor diodes and an inductor, as shown in Figure 5.22(a). The LC oscillator resonates at an angular center frequency of

$$\omega_c = \frac{1}{\sqrt{LC_{tot}}}, \tag{5.20}$$

where L is the parallel inductance, and C_{tot} not only consists of a variable capacitance, C_{var}, but it also includes the parasitic capacitances of the inductor, the gate and drain junction capacitance, and the output buffer loading. At this resonant frequency, the reactances of the inductor and the capacitors are equal in absolute value, yielding infinite impedance and thus an infinite quality factor. However, in practice, on-chip inductor

exhibits series resistance (not to mention the parasitics of varactor) due to the metal wires. The equivalent impedance of the lossy LC tank is given by

$$Z_{eq}(s) = \frac{R_s + Ls}{1 + LC_{tot}s^2 + R_sC_{tot}s}, \tag{5.21}$$

where R_s is the series resistance. This suggests that the impedance does not go to infinity at any frequencies, and the circuit has a finite quality factor, which directly deteriorates phase noise performance and output voltage swing.

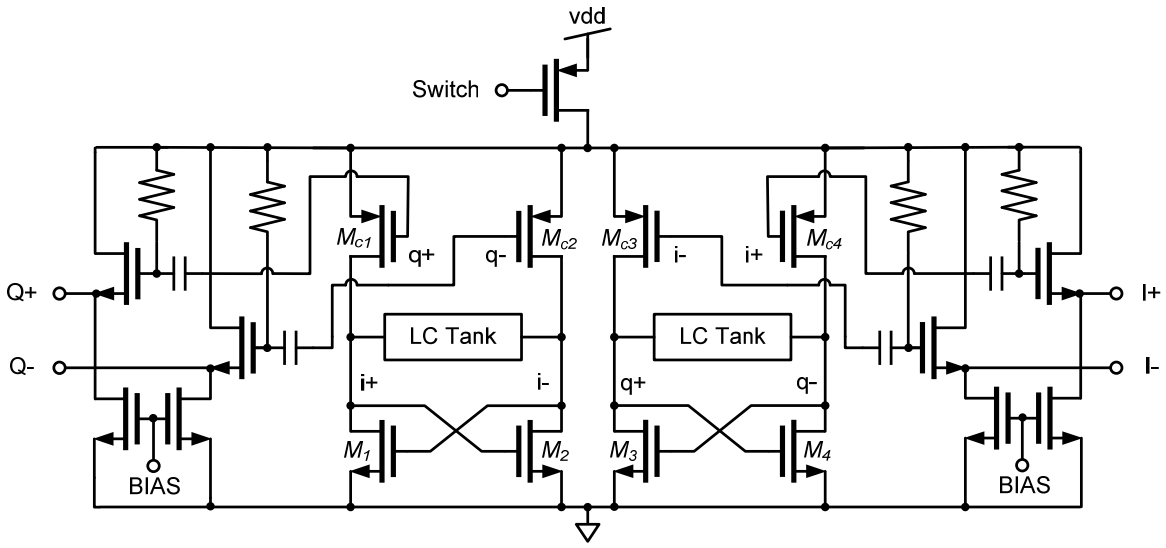

Figure 5.21: Schematic of the 13 GHz QVCO.

The coupling transistor ($M_{c1\text{-}4}$) is responsible for a large contribution to the overall phase noise. The negative resistance of -1/*gm* that the cross-coupled pair (M_1-M_2 and M_3-M_4) presents across the two drain terminals is used to overcome the loss of resonator so

that the resonator can be oscillated. As demonstrated in [88], the most effective way to lower phase noise is to use an LC tank with higher Q and to maximize signal amplitude. A higher inductor-to-capacitor ratio results in the phase domain into a steeper phase roll off at the resonant frequency, which means that the tank rejects stronger any phase deviation. In summary, to achieve low phase noise, inductance and amplitude should be maximized while capacitance and resistance should be minimized at the cost of smaller tuning range.

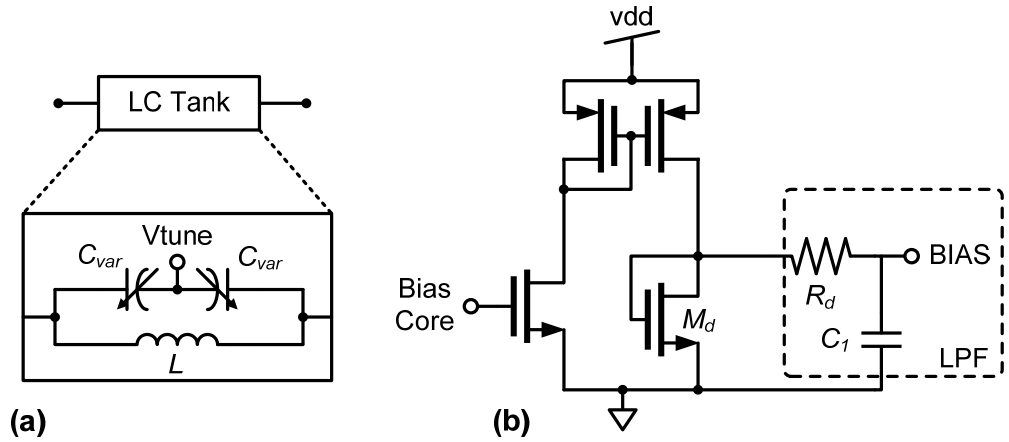

Figure 5.22: (a) LC tank; (b) Schematic of the bias circuit for QVCO output buffer.

The switching operation of the coupling transistor up-converts the 1/f noise to the resonance frequency, resulting in phase noise degradation. The rule of thumb is: for good phase noise, the coupling transistor should be sized smaller or the cross-coupled pair should be sized larger; for small phase error, the coupling transistor should be larger or the cross-coupled pair is sized smaller [86]. This implies that minimizing the phase noise

does not improve the phase error since they contradict each other. According to the SpectreRF simulation, the diode transistor, M_d, from the bias circuit, as shown in Figure 5.22(b), contributes 70% of the spot noise to the QVCO core. A low-pass filter is designed to suppress the flicker noise that contributes to the carrier phase noise. The noise contribution decreases 35%, which is about the same as the noise generated by the individual cross-coupled pairs, and the simulated phase noise at 1 MHz improves by 2 dB. Considering the trade-off between phase error and noise, the ratio of cross-coupled pair to coupling transistor is chosen 3 to 1. Figure 5.23 shows 50 Monte Carlo simulation results of relative I/Q phase mismatch. All the trials fall within ±3 degrees deviation from the ideal 90 degrees between the differential I/Q outputs.

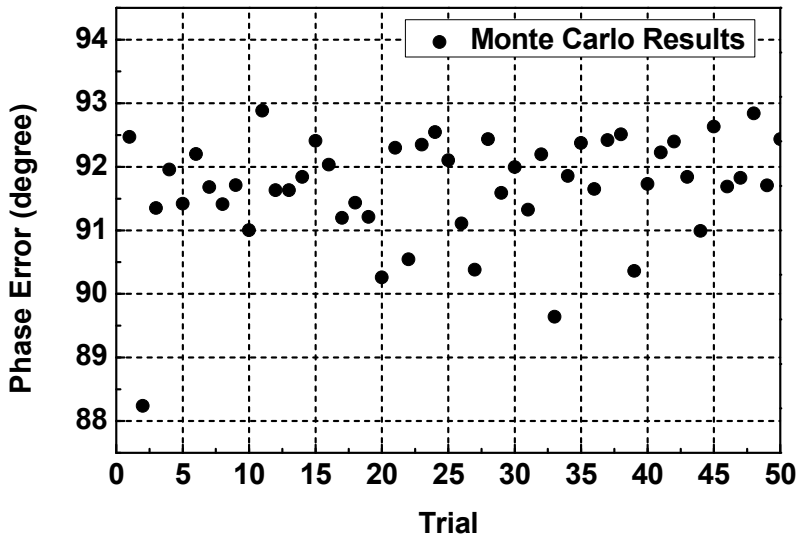

Figure 5.23: QVCO phase error between I/Q outputs.

The QVCO is first characterized separately on a test structure, occupying an area of 900 µm x 500 µm, as shown in Figure 5.24(a). In Figure 5.24(b), the free-running QVCO exhibits a tuning range from 12 GHz to 14 GHz. The K_{VCO} in the center of tuning voltage is 2.9 GHz/V and has a phase noise of -95 dBc/Hz at 1 MHz offset. The overall power consumption is 15 mW from a standard 1 V supply.

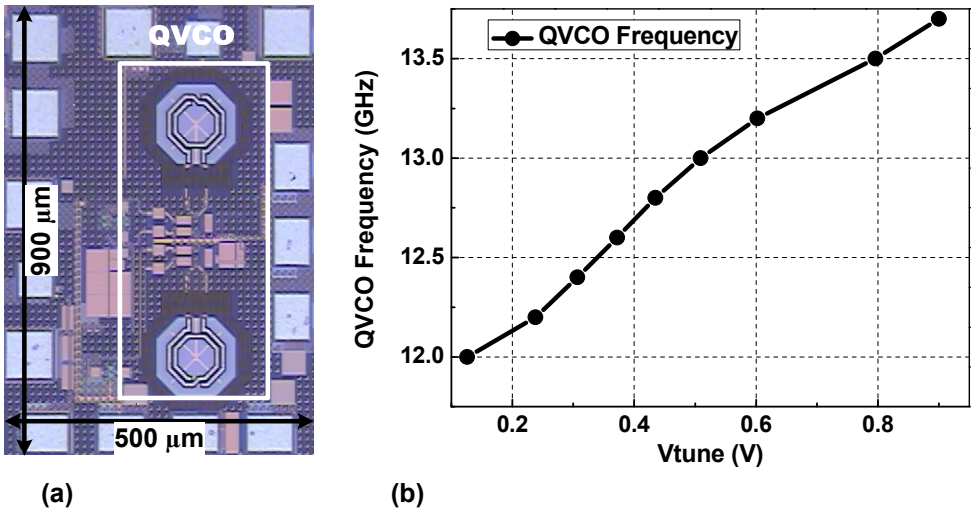

Figure 5.24: (a) Microphotograph of the QVCO test structure; (b) Measured oscillating frequencies at various tuning voltages.

5.3.5.2 Double-Balance Passive Mixer

The input to the quadrature demodulator is a modulated IF carrier and is down-converted to baseband frequency. The conventional double-balanced Gilbert-cell mixer, shown in Figure 5.25(a), is not suitable for 1 V operation due to the trade-off between linearity and conversion gain [28]. Since the maximum allowable output swing directly

depends on the available voltage headroom across the output load resistor given that the RF transistors need to be in the saturation region, a conventional mixer pays the penalty for low conversion gain, consequently poor linearity. Therefore, the double-balanced passive mixer in Figure 5.25(b) utilizes a passive mixing core of RF transistors followed by a differential output buffer to compensate the conversion loss due to passive mixing. Linearity is preserved in this design because the output buffer requires only two-transistor stacking. The mixer provides a conversion gain of 3 dB with a bandwidth greater than 4 GHz and has a power consumption of 3 mW.

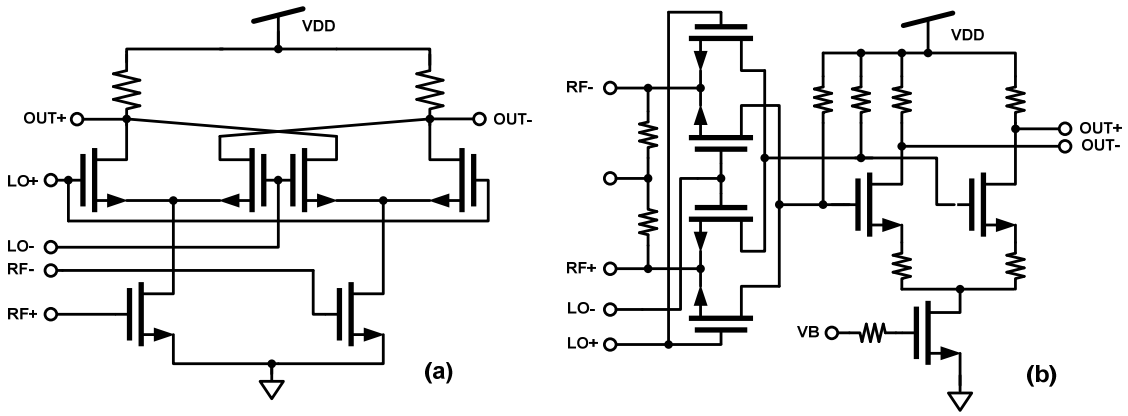

Figure 5.25: (a) Schematic of the double-balance Gilbert mixer; (b) Schematic of the double-balanced passive mixer.

5.3.5.3 Baseband Amplifiers

The baseband VGAs in each I and Q path are implemented with AGC and DC offset compensation loops, as shown in Figure 5.26. Each of the quadrature signal paths

consists of three cascaded amplifiers to provide a maximum gain of 24 dB with a continuous gain variation of 27 dB.

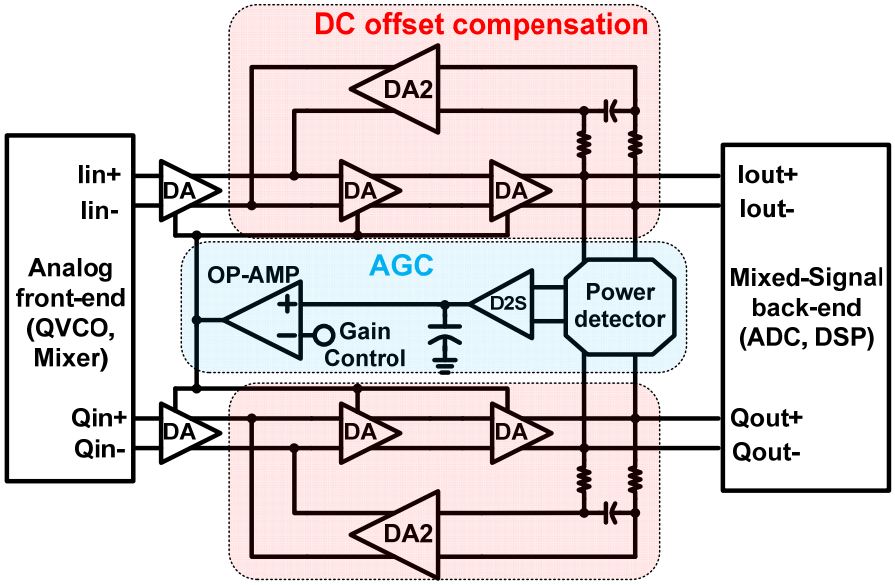

Figure 5.26: Block diagram of the VGA with AGC and DC compensation.

The schematic of one VGA is shown in Figure 5.27(a). Its gain variation and high linearity are achieved using variable source degeneration. Since the VGAs are high-gain amplifiers, any experienced DC offset in the path would lead to erroneous calculations for subsequent quantizers. Therefore, a DC offset compensation feedback loop is required to minimize this offset. It is achieved by connecting the differential output of the third VGA in opposite polarity to the differential output of the first VGA in a low-frequency feedback loop. The accuracy of the DC offset compensation depends on the voltage gain of the differential amplifier, and its schematic is shown in Figure 5.27(b).

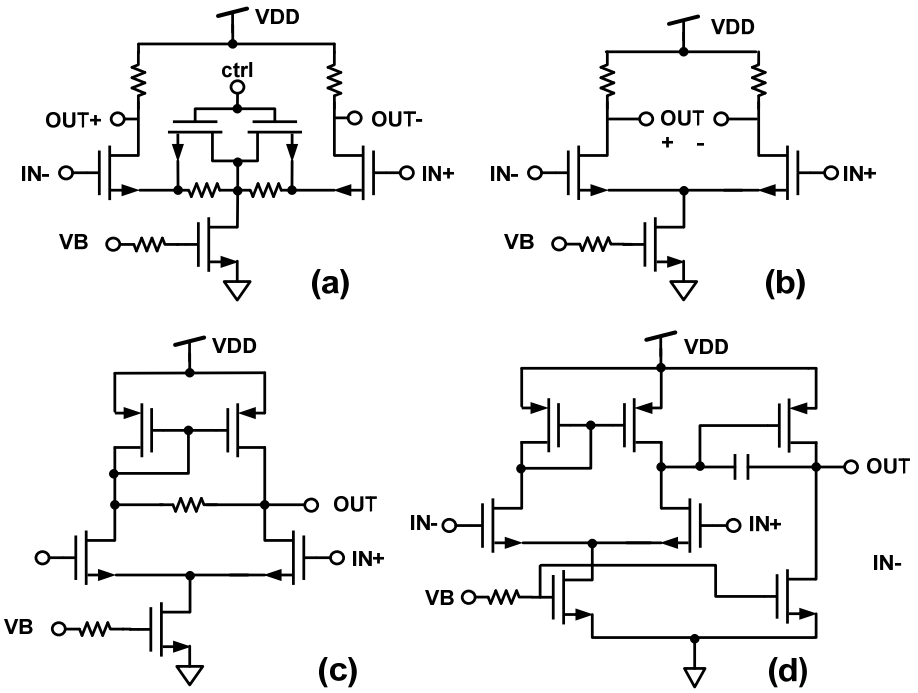

Figure 5.27: (a) Variable-gain amplifier schematic; (b) Differential amplifier schematic; (c) Differential-to-single-ended amplifier schematic; (d) Operational amplifier schematic.

To avoid clipping distortion to the baseband ADCs, AGC is required to maintain the VGAs output power constant. It can be realized using a power detector, a differential-to-single-ended amplifier, a LPF, and an operational amplifier (op-amp). The schematics of the differential-to-single-ended amplifier and op-amp are shown in Figure 5.27(c) and Figure 5.27(d), respectively. For faster settling response, the cut-off frequency is chosen in the low megahertz range. The output power of the VGA can be digitally controlled and set to a desired value through a 6-b current-steering DAC. The total power consumption of the baseband VGAs with AGC and DC compensation is 30 mW.

5.3.5.4 Digital-to-Analog Converter

The input to the 5-bit DAC is the digitized error signal from the high-speed DSP implemented using standard-cell ASIC flow. The schematic of the current-steering binary-weighed R-2R 5-bit DAC is shown in Figure 5.28. This architecture uses inverters to sum the current in each order path and convert to voltage domain. The DAC can be easily analyzed using Thevenin-equivalent resistance method to calculate each distinct level. The inverters driver is designed for low on-resistance, so the static linearity of ladder network is not degraded when the DAC switches from "10000" to "01111". The advantage of this topology is its insensitivity to parasitic capacitance and therefore is fast.

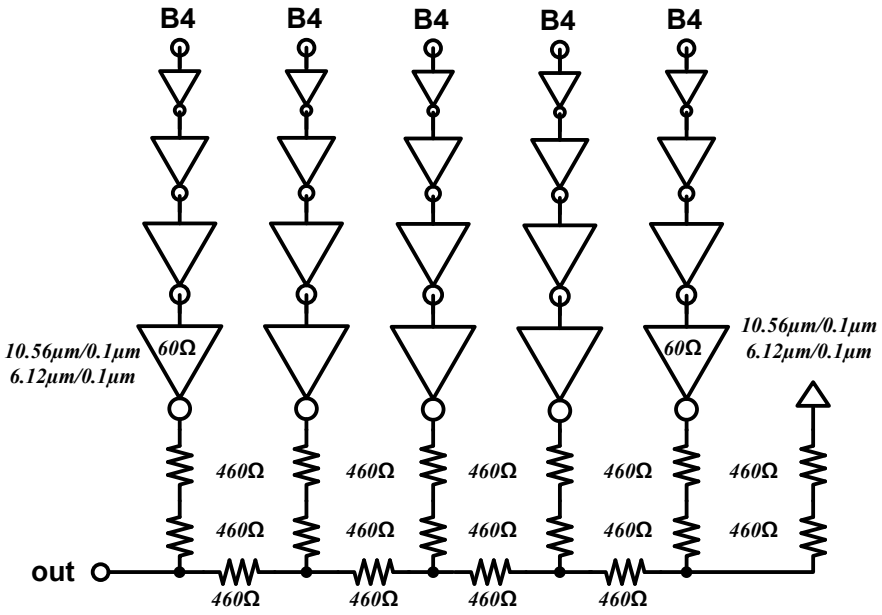

Figure 5.28: Schematic of the high-speed 5-bit DAC.

The maximum operating frequency is mainly governed by the resistor value in R-2R ladder network and the specific load, which is the input capacitance of the error amplifier. As a result, such *RC* configuration limits high-speed operation if one of those parameters is not optimized. Considering a loading of 50 fF and resistance of 500 Ω, the output 3 dB bandwidth is calculated to be 6.37 GHz.

5.3.5.5 Error Amplifier and Loop Filter

The output of the high-speed DAC feeds to an error amplifier consisted of two source follower stages, as shown in Figure 5.29. Since the source follower buffers are complementary, and utilize *PMOS* and *NMOS* transistors, the DC voltage between input and output ports are relatively close. As discussed in the QVCO section, a wide frequency tuning range from 12 GHz to 14 GHz suggests that excessive loop gain in a closed-loop system could lead to instability. Therefore, source follower stages are implemented to provide a voltage loss of 10 dB. Following the EA, the loop filter serves three purposes: provide an anti-aliasing filter after the DAC, filter out noise and high frequency components in *Vtune* line, and loop stability control parameter. The TF of the loop filter is expressed as

$$H(s) = \frac{1 + sC_1R_1}{1 + sC_1R_1 + sC_2R_1}, \tag{5.22}$$

where C_1 is the parallel capacitor, R_1 is the parallel resistor contributing to both pole and zero, and C_2 is the shunt capacitor. As the input power of the BPSK modulated signal

increases, or the voltage swing of the error signal becomes larger, the pole frequency location should be lower for stability concern. This can be achieved by increasing the capacitor value, C_2, or the resistor value, R_1.

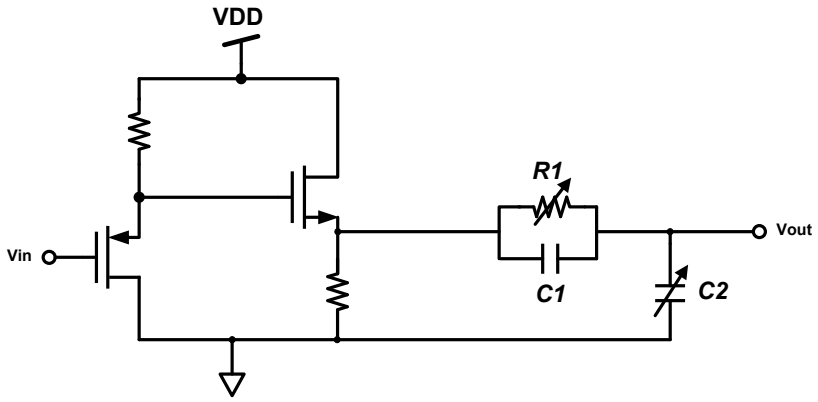

Figure 5.29: Schematic of the error amplifier and loop filter.

5.4 Measurement Setup

Figure 5.30 shows the measurement setup of the mixed-signal demodulator. For measurement purposes, the chip is mounted onto a FR-4 based module using wirebonding. The measurement setup modulates either an uncompressed HDMI video streaming or PRBS pattern generator with the 13 GHz LO through the off-the-shelf I/Q mixer followed by a 30 dB attenuator. Then, the single-ended modulated signal is converted to differential signals through a 180 degrees hybrid to feed the mixed-signal quadrature receiver with a modulated signal. The data output is measured by a signal

integrity analyzer for eye-diagram captures. In addition, it is connected to a high definition TV featuring a real-time uncompressed video streaming.

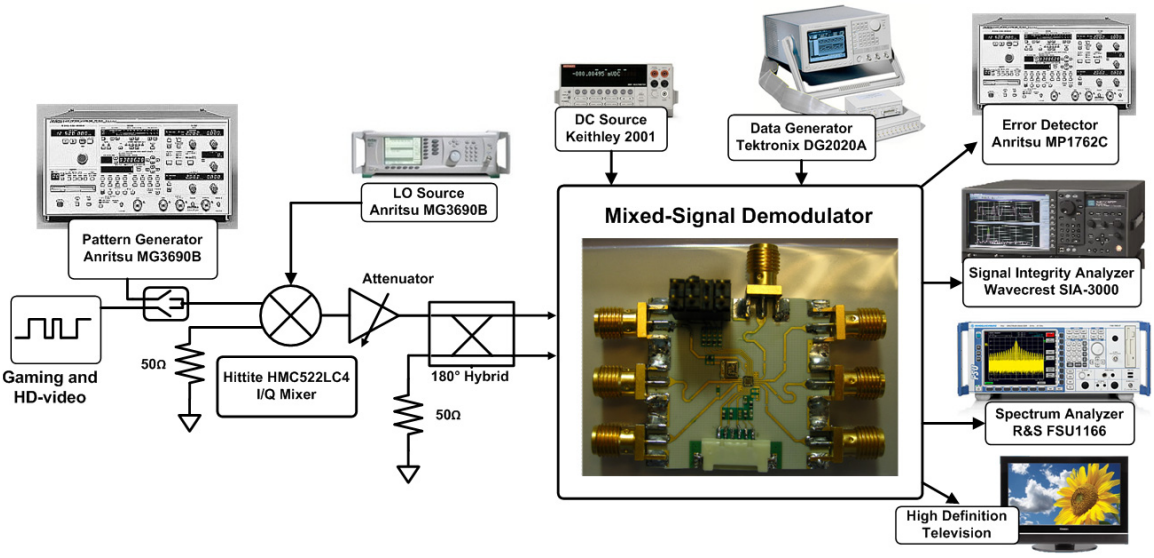

Figure 5.30: Measurement setup of the mixed-signal demodulator.

5.5 Measurement Results

The quadrature receiver chip is fabricated using a standard 90 nm digital 1P7M CMOS process and occupies an area of 1.19 mm x 1.275 mm, as shown in Figure 5.31(a). A HD video streaming experiment is also performed to test the stability of the proposed mixed-signal demodulator, and its setup is shown in Figure 5.31(b). The HDMI source (i.e., Microsoft Xbox 360) is first serialized using a HDMI-to-SDI converter at an uncompressed data rate of 1.485 Gbps, and the resulting bitstream modulates the 13 GHz carrier using the off-the-shelf I/Q mixer in the same manner, as seen in Figure 5.30. Since

the demodulated output contains a differential signal, the positive net is connected to a SDI-to-HDMI converter, and the negative net is connected to either a bit-error detector or a signal integrity analyzer.

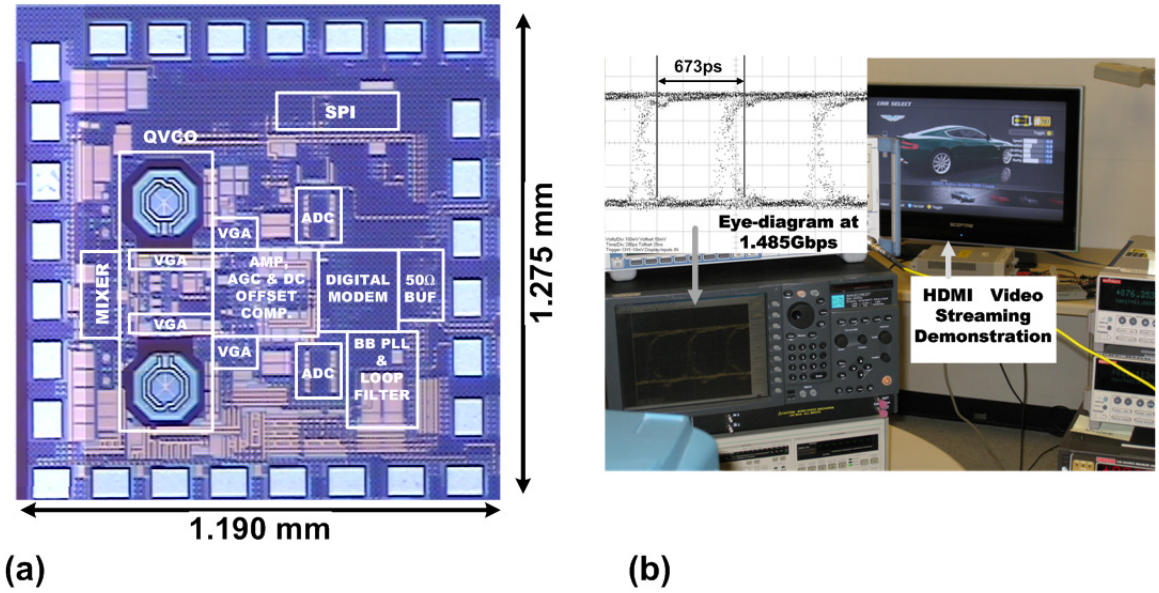

Figure 5.31: (a) Microphotograph of the mixed-signal demodulator; (b) Real-time HDMI video streaming demonstration.

Figure 5.32(a) shows the gain response of the analog path with and without DC offset compensation at various IF frequencies. The lines with circle symbols indicate the analog gain at different IF frequencies in Q-path. Similarly, the analog gain of the I-path is labelled with square symbols. The maximum measured gain with DC offset compensation is 26 dB at the center of the designed local oscillating frequency, and achieves a double sideband bandwidth of 2.4 GHz. The I/Q gain imbalance is further plotted in Figure 5.32(b). This is derived by subtracting the measured gain in the I-path

by the gain in the Q-path. When the DC offset compensation is enabled, the gain difference between I and Q channels is less than 1 dB across all baseband frequencies. From 750 MHz to 3 GHz, the gain imbalance is even less than 0.4 dB. On the other hand, when the DC offset compensation is disabled, the I/Q gain mismatch can be as high as -4 dB at a baseband frequency of 500 MHz. As expected, the gain mismatch attenuates at higher baseband frequencies.

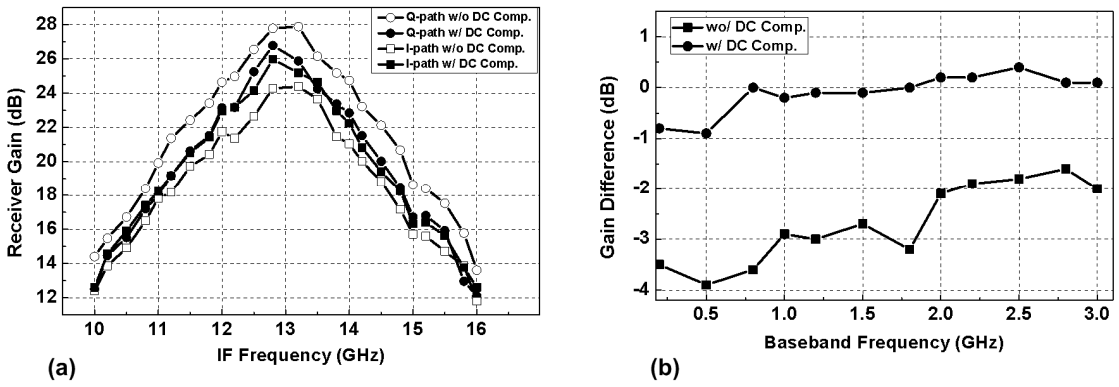

Figure 5.32: (a) Measured down-conversion gain versus IF frequencies; (b) I/Q gain imbalance versus baseband frequencies.

The AGC system is next characterized. Figure 5.33(a) shows an input dynamic range from -44 dBm to -17 dBm with a measured baseband power level from -16 dBm to -3 dBm at various closed-loop gain setting. In the operation of DSP, the baseband power level is set to -10 dBm, which corresponds to a 200 mVpp voltage swing at the input of ADC. The coherent BPSK demodulator performance is then characterized. Figure 5.33(b) displays the sensitivity of the mixed-signal demodulator by varying the input DC voltage

of the ADCs in both I and Q channels together. This test is conducted using a 2^{31}-1 PRBS signal at a data rate of 1.485 Gbps for an input IF power level of -33 dBm. The demodulator is robust against the DC bias variation and remains error-free demodulation from the ADC input bias voltages of 465 mV to 555 mV.

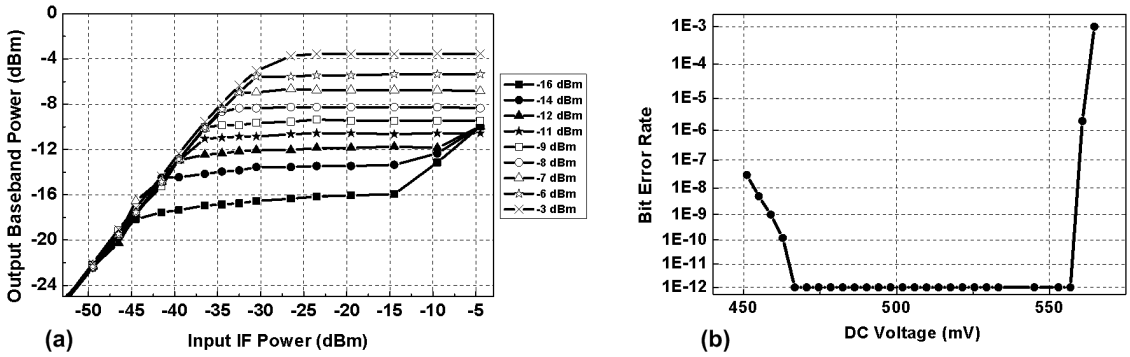

Figure 5.33: (a) Measured baseband power level at various AGC setting; (b) Measured BPSK BER versus ADC input bias at 1.485 Gbps.

Furthermore, a measured minimum sensitivity is shown in Figure 5.34. Wide synchronization ranges occur at higher input IF power levels. When the input IF power level is sufficiently strong (i.e., > -33 dBm), the synchronization range is better than 40 MHz. At -39 dBm power level, the range drops down to only 20 MHz. It should be noted that the BER is not affected at saturated baseband power level and maintains error-free demodulation up to 2.5 Gbps. Therefore, the performance will not deteriorate if the gain of AGC loop is set to maximum. Hence, the dynamic range of the demodulator is greater than the 27 dB provided by the AGC and better than 33 dB. In Figure 5.34(b), the synchronization ranges with corresponding BER are measured at various data rates from

432 Mbps to 3.5 Gbps. This DSP achieves synchronization range of 51 MHz at 864 Mbps and 15 MHz at 3.5 Gbps, respectively. In the same plot, error-free data transmission is maintained up to 2.5 Gbps data rate, and 1E-09 up to 3 Gbps. The highest achieved operating data rate is 3.5 Gbps with a BER better than 1E-08 measured at an input power level of -33 dBm.

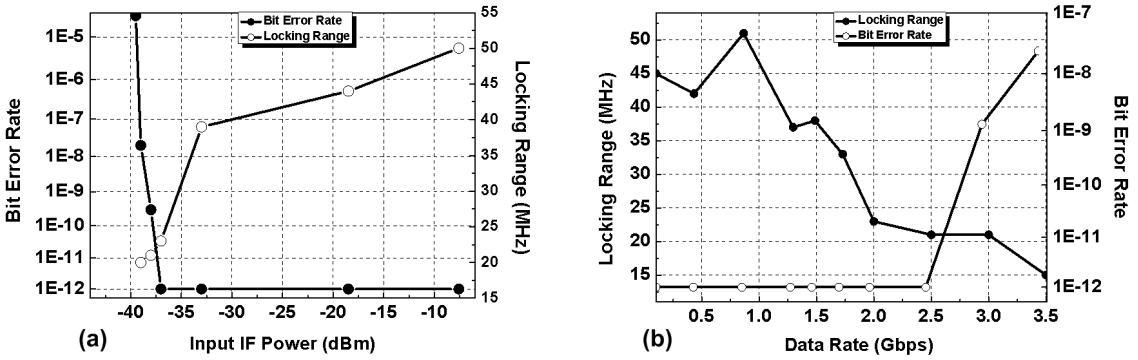

Figure 5.34: (a) Minimum sensitivity of the BPSK demodulator at 1.485 Gbps; (b) Locking range and BER versus data rates.

The demodulated eye-diagrams for 1.485 Gbps and 2.5 Gbps data rates are shown in Figure 5.35(a) and Figure 5.35(b), respectively. The ripples on those eye-diagrams indicate a significant noise contribution generated from the switching activity of baseband digital circuits to the supply line. The performance summary of the mixed-signal demodulator is shown in Table 5.3. The overall power consumption is 60 mW including 52 mW from the analog front-end and 8 mW from the ADC/DSP/DAC.

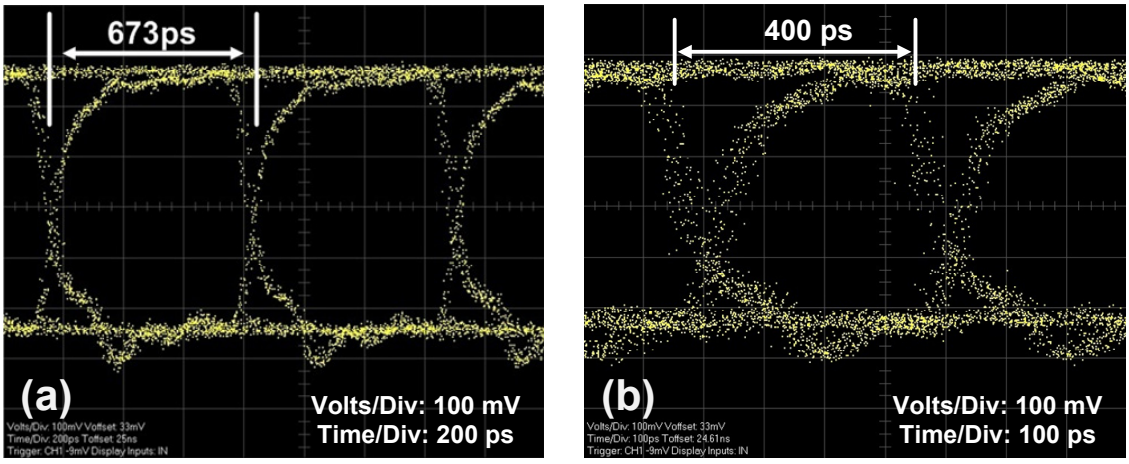

Figure 5.35: (a) Demodulated eye-diagram at 1.485 Gbps; (b) Demodulated eye-diagram at 2.5 Gbps.

Table 5.3: Performance summary of the coherent mixed-signal demodulator.

Specification	Parameter		Unit
Supply voltage	1		V
Power consumption	60		mW
	Analog	Digital	—
	52	8	mW
Error-free transmission	2.5		Gbps
Maximum speed	3.5		Gbps
Dynamic range	> 33		dB
Minimum sensitivity	-39		dBm
Maximum locking range	51		MHz
Bit-error rate	< 1E-12 up to 2.5 Gbps		—
	< 1E-09 up to 3.0 Gbps		—

5.6 Summary

In this chapter, a broadband quadrature demodulator with an embedded high-speed mixed-signal converter in 90 nm CMOS technology is presented, which leverages unique boundaries between analog and digital circuits to realize a high-performance IC

design with compact area and low-power dissipation. A high-speed digital ASIC chip integrated with analog front-end is successfully demonstrated, and performs the desired multi-gigabit demodulation operation. The proposed architecture presents a fully-integrated system that simultaneously achieves multi-gigabit modem functionality and maintains the overall power budget in sub-Watt regions. With a minimum sensitivity of -39 dBm and a dynamic range of 32 dB, the mixed-signal demodulator can perform a multi-gigabit BPSK demodulation up to 2.5 Gbps error-free transmission. This demonstrates for the first time a unique multi-gigabit solution for low-power millimeter-wave (60 GHz, 70-80 GHz) radios.

CHAPTER 6

HIGH-PERFORMANCE DUAL-MODE DEMODULATOR

6.1 Introduction

This chapter introduces a complete high-performance dual-mode multi-gigabit demodulator with an emphasis to utilize the entire available 7 GHz spectrum in the license-exempt 60 GHz band. To occupy the spectrum completely, a high-performance demodulator is designed and targeted to demodulate a BPSK signal up to 3.5 Gbps error-free transmission. In order to satisfy this stringent speed requirement while maintaining power consumption low, an optimized high-speed ADC design is developed. Two-channel time-interleaved architecture is also employed throughout digital back-end to achieve 6.912 GS/s. In addition, an ASK demodulation technique is investigated and implemented along with the coherent BPSK demodulator. Circuit implementation and analysis to realize high-performance ADC and demodulator are discussed in this chapter.

6.2 High-Performance 3-bit Flash A/D Converter

6.2.1 Architecture

Figure 6.1 shows the block diagram of the high-performance 3-bit ADC. Unlike the ADC design in previous chapter, this ADC is upgraded to fully-differential operation for the following benefits. A fully-differential input provides good dynamic common-

mode rejection and doubles the dynamic range. Inherently, SNR increases and thereby has superior DC and AC common-mode rejection. The first ADC building block, T/H circuit, improves resolution bandwidth at high frequencies and reduces kickback noise from the array of comparators. The T/H circuit also employs a common-mode feedback to cancel the voltage imbalance from its pseudo-differential output. Following the T/H circuit, nine differential amplifiers (preamplifiers), including two dummies at the boundary, are designed to largely cancel out even-order distortions. The dummy preamplifiers are used to compensate the edge effect due to averaging network. Each dummy preamplifier drives the averaging network by comparing the analog input signal with uniformly spaced threshold voltages that extend beyond the actual full scale. When the resistive averaging network is properly designed, the impact of the random static offsets on both preamplifiers and comparators is alleviated, allowing smaller devices size for higher analog bandwidth. The preamplifiers array senses the difference between the sampled differential input signal and the differential threshold, generated by voltage references, to drive nine comparators (Comparator I), followed by another resistive averaging network. The middle seven of these nine comparator outputs connect to two pipelined latch stages. Increasing the comparator settling time reduces the metastability error due to the inadequate regeneration time constant in the comparator. This type of error can only be suppressed by the suggested method in order to maintain the same clock speed. Finally, the binary thermometer output codes are converted to gray codes and then binary codes. To realize a robust ADC design, programmable bias control and resistive reference voltage trimming are implemented in case of insufficient analog bandwidth or internally corrupted SNR.

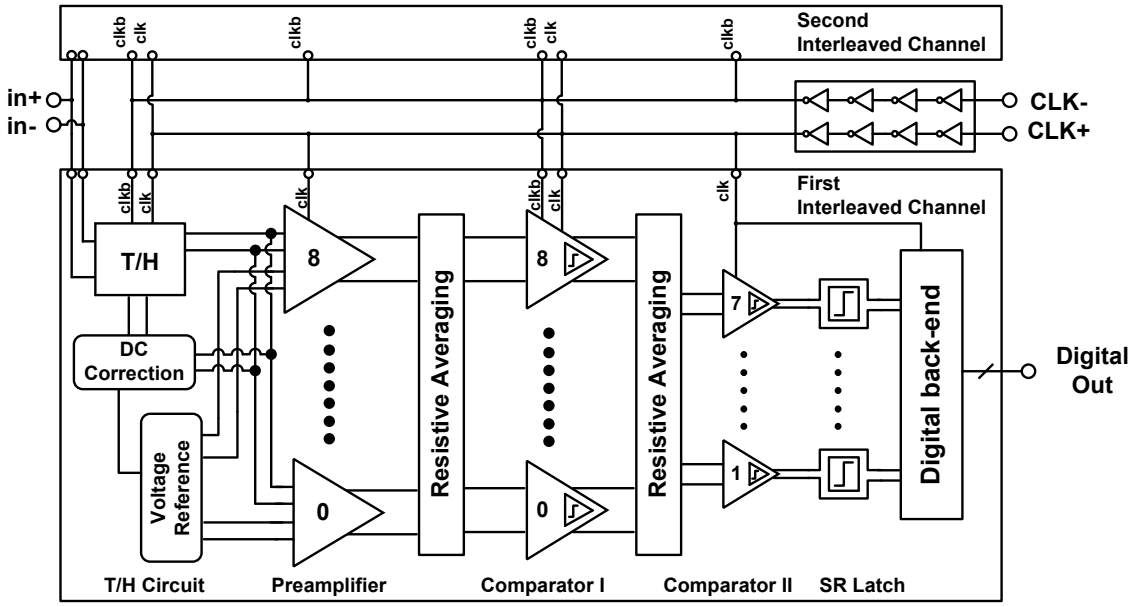

Figure 6.1: Block diagram of the high-performance 3-bit ADC.

Dynamic inaccuracies due to clock skews distributed across the array combined with clock jitter are serious issues in high-speed data conversion. Without two-channel interleaving, the clock skews due to the imbalanced loading are inevitable at high frequencies. By time-interleaving two identical ADCs and minimizing area, the effective capacitive loading seen by the differential clock source is the same, and the sampling rate is double. Detailed timing diagram of the clock source to each stage and the clock buffer sizing are shown in Figure 6.2. To avoid race condition, the clock signal is fed to the individual building block in reverse and finally to the front-end T/H circuit. The target sampling rate of 6.912 GS/s implies that each ADC channel is effectively sampling at a frequency of 3.456 GHz. To realize a high-speed digital encoder in 90 nm CMOS process, heavily pipelining between the combinational logics is needed. As a result, the

thermometer-to-binary encoder requires nine clock cycles to convert an analog sampled voltage. The latency of the complete high-performance ADC is eleven cycles, including two additional cycles in the T/H circuit, preamplifier, and comparator stages. The only drawback of the converter latency is the reduced synchronization range of the mixed-signal coherent BPSK demodulator, as discussed in the previous chapter.

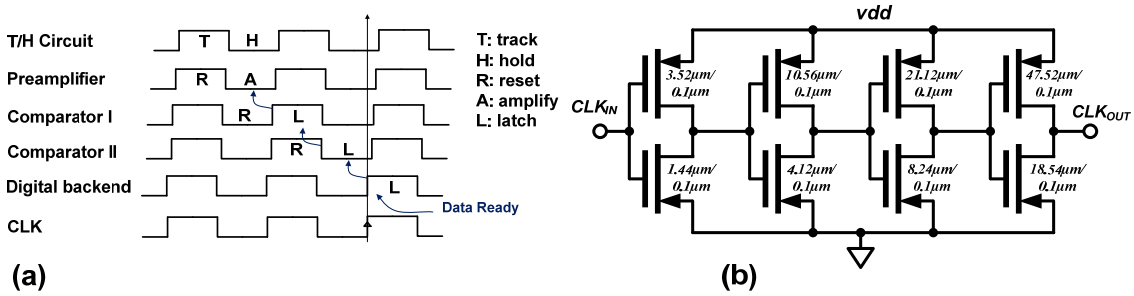

Figure 6.2: (a) Timing diagram of the clock source to each stage; (b) Clock buffer schematic.

6.2.2 Track-and-Hold Circuit

6.2.2.1 Design Considerations

Owing to inherent clock jitter and device mismatch, the sampling instants of ADCs may differ slightly, especially in the gigahertz operating frequency regime. To improve the dynamic performance of an ADC, T/H circuit is implemented to provide a stable input level so that the preamplifiers in parallel can compare with all the thresholds in just one clock cycle. This suggests that the T/H circuit must deliver enough current to

charge or discharge a large input capacitance from the preamplifiers. The resulting current driving capability of the T/H circuit is given by

$$I_{T/H} = \frac{f_s \cdot N \cdot C_{in} \cdot V_{fs}}{2\alpha}, \tag{6.1}$$

where f_s is the sampling frequency, N is the number of preamplifiers, C_{in} is the input capacitance of a single preamplifier, V_{fs} is the full-scale range, and α is the fraction of the clock period to settle a tracked input [56]. Considering a clock rate of 4 GHz, $N = 9$, $C_{in} =$ 10 fF, $V_{fs} = 200$ mV, and $\alpha = 0.05$, the required current consumption of the T/H circuit is 720 μA. Therefore, the designed T/H circuit consumes more current than the calculated value for PVT consideration.

Figure 6.3 shows the schematic of the T/H circuit. As the supply voltage is limited to 1 V, the sampling switches become problematic because the switch on-resistance does not stay constant across the full-scale input range due to the nonlinear body effect, and therefore *RC* delay varies. The input-dependent on-resistance during track mode also causes nonlinearity and distorts the track-mode current flowing into the hold capacitor at high frequencies. This phenomenon only gets worsened at low supply voltage or high input swing. In order to reduce body effect and modulation, the bulk terminal of the source follower *PMOS* transistor is connected to its source terminal. Considering *kT/C* thermal noise, the sampling capacitor is chosen four times larger than the effective nonlinear capacitance at node *Vs*. The track-mode distortion due to nonlinear switch on-resistance is alleviated by choosing a low input common-mode voltage, 0.2 V, consisted of only *NMOS* transistors. In addition, the distortion caused by charge injection and clock

feed-through is compensated using a complementary dummy switch at a smaller size. Simulation shows that the T/H circuit, at best, attains -52 dBc track-mode distortion for a single-ended Nyquist input at 0.2 mVpp and 2 GHz. The performance summary of the T/H circuit is shown in Table 6.1.

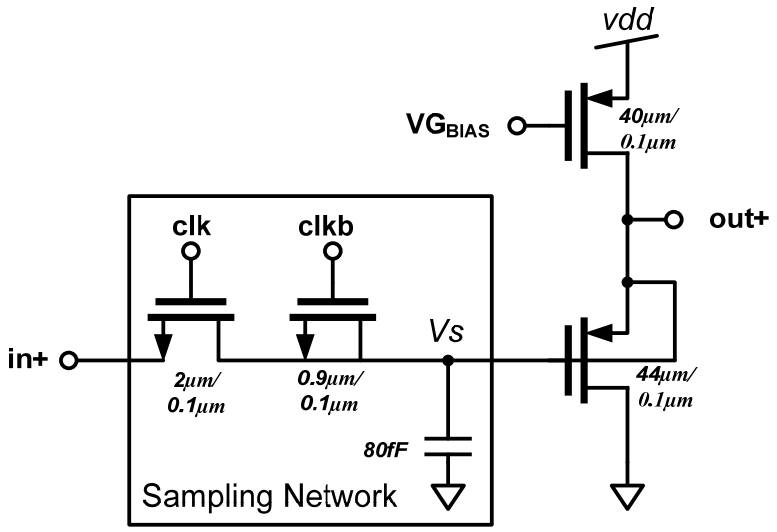

Figure 6.3: Schematic of the T/H circuit.

Table 6.1: Performance summary of the T/H circuit.

Specification	Parameter	Unit
Supply voltage	1	V
Power consumption	0.95	mW
Input common-mode voltage	200	mV
Output common-mode voltage	550	mV
Voltage gain	-1.31	dB
Input 3 dB bandwidth	5.53	GHz
Output 3 dB bandwidth including nine preamplifiers loading and 10 fF wiring	4.9	GHz
3rd order harmonic	-62 @ fin = 250 MHz -52 @ fin = 2 GHz	dBc dBc
Switch on-resistance	240	Ω

6.2.2.2 DC Offset Correction

Due to PVT variations, the output common-mode voltage of the pseudo-differential T/H circuit varies from chips to chips. To establish a stable common-mode voltage, a DC correction circuit, known as the common-mode feedback (CMFB) circuit, is implemented, as shown in Figure 6.4(a). Using a CMFB at the T/H output guarantees that the sampled input voltage falls within the designed reference levels, assuming the AGC preceding the ADC provides a full-scale input. Ideally, the negative input terminal of the op-amp is fixed to *Vref*, which is tapped directly from the middle resistive voltage reference. The common-mode output voltage, *CM voltage*, is extracted using two large resistors in series and connects to the positive terminal of the op-amp. The schematic of the op-amp is shown in Figure 6.4(b), consisted of seven transistors, and it achieves a phase margin of 75 degrees using a Miller compensation capacitor of 1.3 pF at a power consumption of 0.31 mW. Its detailed performance summary is listed in Table 6.2.

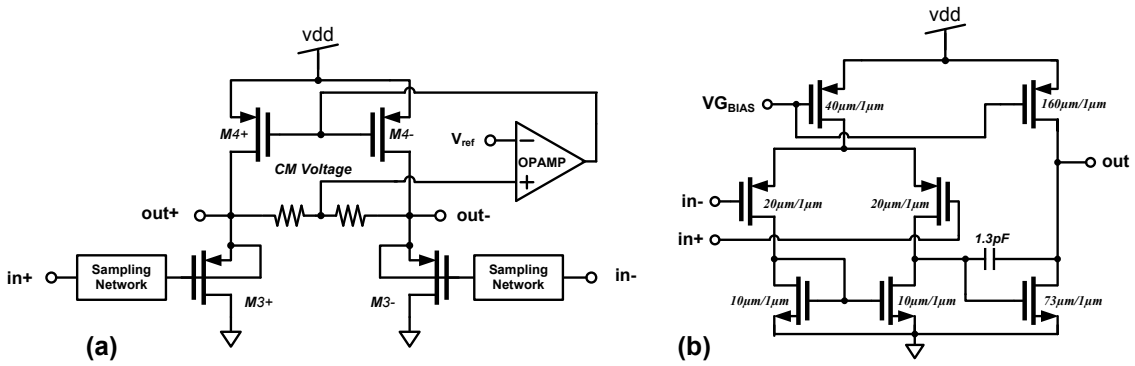

Figure 6.4: (a) T/H circuit with CMFB; (b) Operational amplifier schematic.

Table 6.2: Performance summary of the CMFB op-amp.

Specification	Parameter	Unit
Supply voltage	1	V
Current consumption	310	μA
Voltage gain	66	dB
Phase margin	75	°
3 dB bandwidth	18	KHz
Unity frequency	36	MHz
Input common-mode voltage	500	mV
Output common-mode voltage	487	mV

To emulate one of the worst-case scenarios, slow-slow corner is verified in the Monte Carlo simulation. In Figure 6.5, *Vref* is initially set to 600 mV, and the data arrives at the T/H circuit input after 95 ns. At 40 ns, *Vref* slowly changes from 600 mV to 550 mV, which is the designed middle voltage reference. As seen from the graph, *CM voltage* tracks *Vref* and eventually settles to 550 mV after 65 ns. At 95 ns, when the output is settled to 550 mV, a ramp input is applied at 4 GS/s. From this point beyond, both CMFB and 3-bit ADC are working simultaneously to ensure that the common-mode voltage between the pseudo-differential T/H outputs follows the designed middle voltage reference. After 101 ns, the 3-bit ADC completes the conversion of eight quantization levels at 4 GS/s. To observe the effects of digital switching noise on the analog circuits, digital and analog *VDDs* are shorted together. The *CM voltage* line indicates switching noise and glitches after 95 ns. However, this does not degrade the ADC performance because the peak amplitude is smaller than the designed LSB, 25 mV. In real design, the analog and digital *VDDs* are separated.

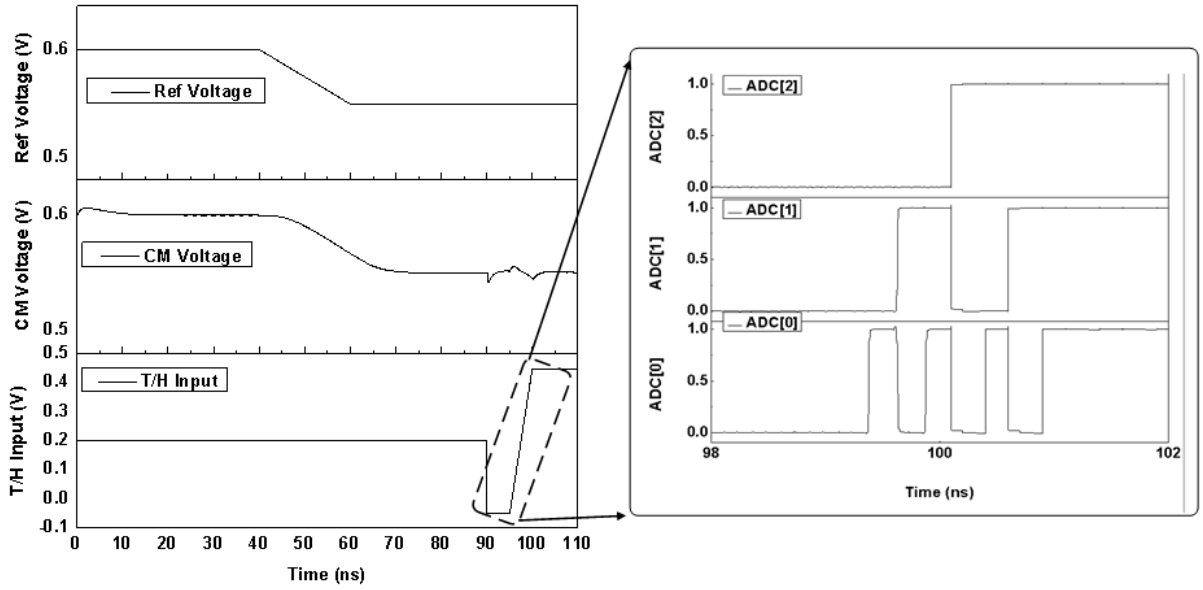

Figure 6.5: Simulation result of T/H circuit with CMFB.

6.2.3 Preamplifier Stage

6.2.3.1 Design Considerations

The preamplifier in Figure 6.6 is the most wideband amplifier in the system mainly to suppress harmonic distortions since the comparator itself is a nonlinear amplifier. The preamplifier is also designed to provide sufficient gain to overcome comparator offsets and to recover large overdrive from one clock cycle. At high frequency, employing a switch transistor at the output node improves overdrive recovery by erasing previous amplification state. To minimize the channel resistance of the reset switch, a low-*Vth* transistor is used.

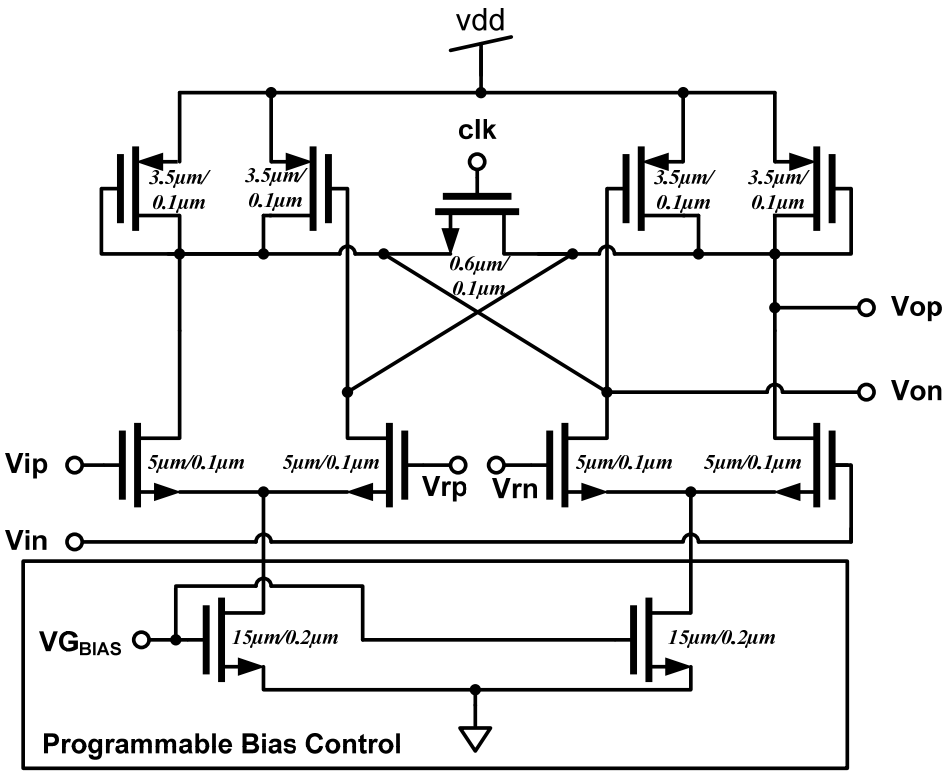

Figure 6.6: Schematic of the preamplifier.

Voltage gain of an amplifier can be boosted by increasing the load resistor value. However, in a low *VDD* design, an increase in load resistor for higher voltage gain lowers the output common-mode voltage, which can unavoidably drive the input differential pair into triode region operation. Another consideration is to use a diode load. Although this is the most linear option, it roughly has a voltage gain of one due to the *gm* cancellation of input transistor and diode load. Connecting the diode in parallel with a cross-coupled *PMOS* pair boosts the gain and biases itself below *VDD-Vth*. The gain is enhanced greatly here because the negative transconductance of the cross-coupled pair cancels the *gm* of the diode, leading to high resistance output.

6.2.3.2 Programmable Bias Control

Since the input data rate varies from 864 Mbps to 3.456 Gbps, a programmable bias control is implemented to accommodate bandwidth and power consumption requirement for different data rates. In Figure 6.7(a), different bias voltages and the corresponding power consumption are plotted. Power consumption varies from 132 µW to 670 µW for six different code setting. Figure 6.7(b) plots the gain and bandwidth variation for different bias voltages. The voltage gain of the preamplifier is independent of the bias voltage because the voltage gain is determined by the *gm* ratio. On the other hand, the 3 dB bandwidth varies from 1.46 GHz to 4.72 GHz due to the technology-dependent GBW. The performance summary of the preamplifier is shown in Table 6.3.

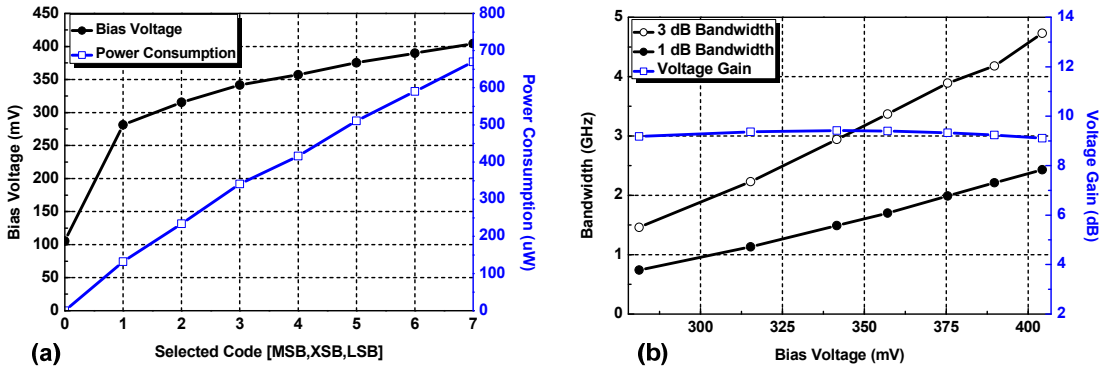

Figure 6.7: (a) Preamplifier bias voltage and power consumption at various code settings; (b) Bandwidth and power consumption of preamplifier at various bias voltages.

Table 6.3: Performance summary of the preamplifier.

Specification	Parameter	Unit
Supply voltage	1	V
Current consumption	415	μA
Voltage gain	1.7 in reset mode 9.4 in amp mode	dB dB
3 dB bandwidth	7.6 in reset mode 3.4 in amp mode	GHz GHz
3rd order harmonic	-43 @ fin = 250 MHz -36 @ fin = 2 GHz	dBc dBc
Input common-mode voltage	550	mV
Output common-mode voltage	496	mV

6.2.4 Comparators Design

Comparator latches implement the function of detecting the zero-crossings. To ensure fast overdrive recovery, differential-input size must be small in addition to using low-*Vth* transistors. The schematic of the first comparator is shown in Figure 6.8(a). Again, the cross-coupled *PMOS* transistors provide gain-boosting negative resistance as well as self-bias from the common-mode feedback. The comparator amplifies the zero-crossing output from the preamplifier when the *NMOS* switch transistor is off (*CLKB* = 0). On the other hand, when the clock goes to one (*CLKB* = 1), the output resets.

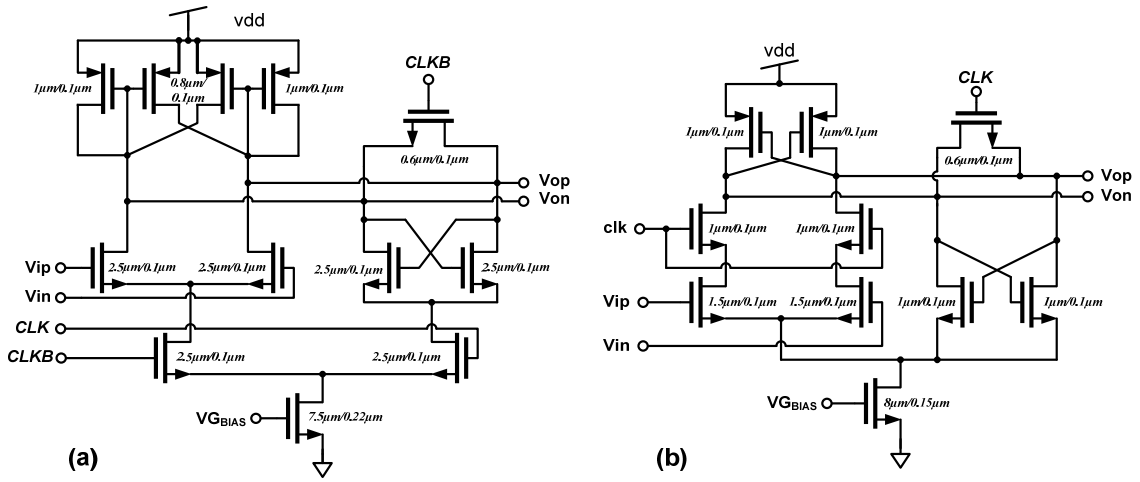

Figure 6.8: (a) Schematic of the first comparator; (b) Schematic of the second comparator.

Using a chain of preamplifier and first comparator, simulation result for overdrive recovery test is shown in Figure 6.9. The comparator resets when *CLK* is low and amplifies the difference at *CLK* = 1. Figure 6.9(a) indicates that the comparator can recover the overdrive from large positive (650 mV) to small negative (547 mV) at 4 GS/s (for illustration purpose, single-ended input swing is displayed). Figure 6.9(b) further shows that the comparator can recover the overdrive from large minus (450 mV) to small positive (553 mV) at 4 GS/s. Since the comparator is essentially a current-mode logic (CML) latch, the propagation delay constitutes sufficient margin to satisfy hold time violation. Setup time violation is not a major issue here because there is no combination logic between the first comparator and the second comparator other than interconnect delay. The performance summary of the first comparator is shown in Table 6.4.

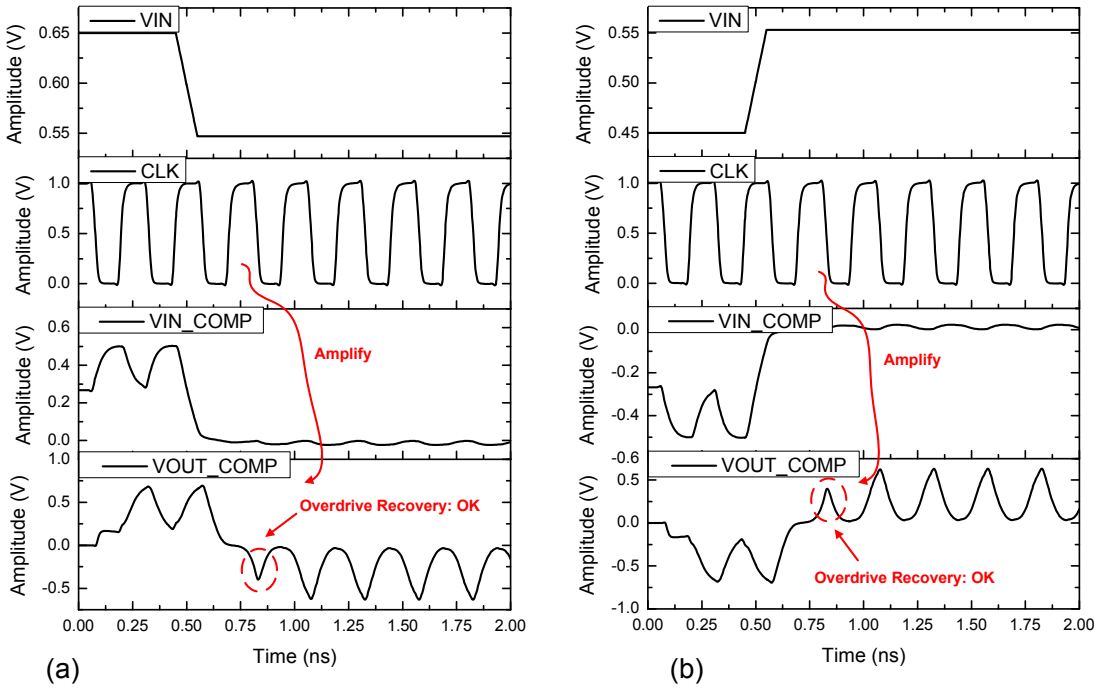

Figure 6.9: (a) Comparator overdrive recovery test from large + to very small -; (b) Comparator overdrive recovery test from large – to very small +.

To reduce BER, two more regeneration stages are added. The schematic of the second comparator is shown in Figure 6.8(b). It consists of a differential *NMOS* pair and positive feedback inverters formed by *PMOS* and *NMOS* cross-coupled pairs. One of the differential input pair discharges the stored voltage and its strength should be strong enough to flip the logic. The second comparator array produces rail-to-rail logic swing for the digital back-end consisting of CMOS SR latch and high-speed encoder. Single-phase clock is applied from this stage throughout digital back-end to accommodate clock skews that could possibly limit the highest clock frequency.

Table 6.4: Performance summary of the first comparator.

Specification	Parameter	Unit
Supply voltage	1	V
Current consumption	99	μA
Voltage gain	2.2 in reset mode 12.5 in amp mode	dB dB
3 dB bandwidth	11 in reset mode 2 in amp mode	GHz
Input common-mode voltage	500	mV
Output common-mode voltage	490	mV
Minimum setup time for 1 LSB	60	ps

6.2.5 Resistor Averaging Network

The accuracy of the transistors is the main limitation to increase the resolution of ADCs as the supply voltage reduces in deep sub-micron CMOS process. To ensure no missing codes and monotonicity, the offset averaging network can be treated as spatial low-pass filters to remove as much as possible the errors and preserve the ideal zero-crossing of the input signal without increasing transistor size [89], [90], [91].

6.2.5.1 Offset Averaging Network as Spatial Filter

Figure 6.10(a) shows the resistive averaging network of three amplifiers each with load resistor R_0. Averaging effect is obtained by coupling the outputs of adjacent amplifiers with average resistor R_1. As long as the amplifiers are operating in the linear range, the zero-crossing amplifier sees a much bigger device with a size equal to the sum of the areas of all active linear amplifiers in the array [90], [92]. As a result, the reduction in static offset voltage compared to a non-coupled differential amplifier is approximately

equal to square root of the number of linear active amplifier stages contributing to the output signal of the zero-crossing stage.

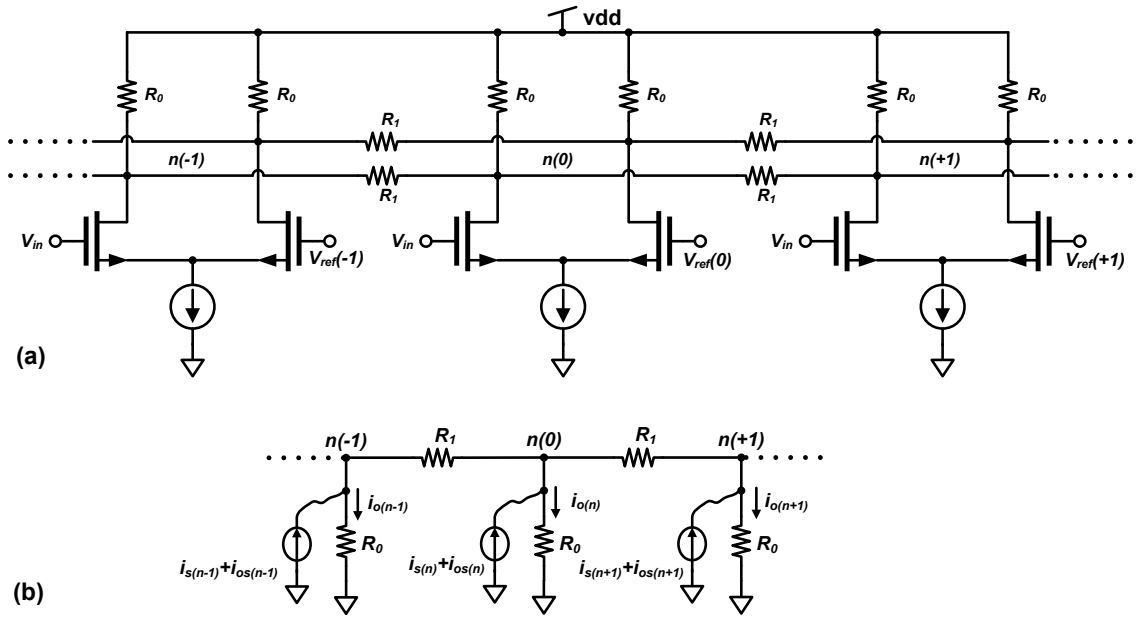

Figure 6.10: (a) Resistive averaging network; (b) A first-order single-ended model under stimulation of small-signal signal and noise currents.

Since the output of differential amplifiers array spreads through lateral connections in the averaging, the impulse response (IR) of the spreading network forms a spatial filter [50], [89], [90], [91]. In Figure 6.10(b), the current, i_o, flowing in each R_0 defines the filter output in response to stimulus from the input differential pair and the tail current source. Ideal current samples will be affected by random errors, which can be seen as spatially distributed white noises. An array of differential pairs injects two different types of stimuli current in the averaging network: signal current and noise

current due to transistor random offset. Consider an input voltage, V_{in}, equal to the threshold voltage, $V_{ref(0)}$, at node $n = 0$. Ideally speaking, the differential current flowing into R_0 at its output zero-crossing should be zero. However, when offset currents, $i_{os}(n)$, are present, noises couple into the spatial filter. Offset currents arise from the mismatch in differential pairs and the fluctuations in the tail currents of zero-crossing generators. The offset currents can be expressed as

$$i_{os}(n) = gm(n) \cdot V_{os}(n) + \Delta I_{tail}(n), \tag{6.2}$$

where $gm(n)$ is the transconductance, $V_{os}(n)$ is the input equivalent offset voltage, and $\Delta I_{tail}(n)$ is the tail-current mismatch of the *nth* amplifier. Figure 6.11(a) illustrates the noise current contribution at each zero-crossing generator.

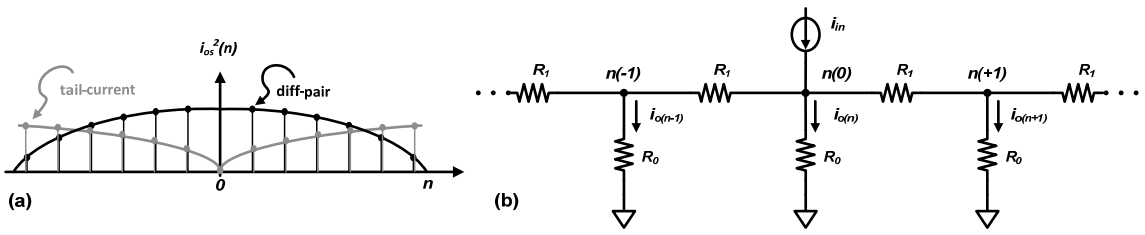

Figure 6.11: (a) Error current injected into averaging network; (b) Amplifier and averaging network modeled as a spatial filter.

If the amplifier input located in the center ($n = 0$) is balanced ($V_{in} = 0$), the error current caused by the differential pair mismatch reaches maximum, while the tail-current mismatch does not cause error current. If the lateral resistor, R_1, is absent, the input-referred offset voltage is essentially equal to $V_{os}(n)$. Averaging resistor allows the offset

currents to flow into R_0 from the adjacent linear zero-crossing generators [51], [89]. On the other hand, when the amplifier in the center of array is clipped, meaning V_{in} is far away from $V_{ref}(0)$, the mismatch in tail-current contributes the most error current.

The IR of the spatial filter can be obtained by applying a unit impulse current at node n and finding the resulting output currents, as shown in Figure 6.11(b). For the sake of simplicity, the following spatial filter analysis is based on first-order resistive network, where the stimuli take forms in current domain. For an error current, i_{in}, injected to an arbitrary node n, Kirchhoff's current law (KCL) requires that

$$i_{in} - i_o(n) - 2 \cdot i_o(n) \cdot \frac{R_0}{R_1} + i_o(n-1) \cdot \frac{R_0}{R_1} + i_o(n+1) \cdot \frac{R_0}{R_1} = 0\,, \tag{6.3}$$

where n represents the index of differential pair in the array, $i_o(n)$ is the output current flowing into node n, $i_o(n+1)$ and $i_o(n-1)$ are the output currents flowing into adjacent nodes $n+1$ and $n-1$, respectively, R_0 is the load resistor, and R_1 is the averaging resistor. Using Z-transform, (6.3) is represented as

$$H(z) = \frac{I_o(z)}{I_{in}(z)} = \frac{1}{1 + 2 \cdot \frac{R_0}{R_1} - (z^{-1} + z) \cdot \frac{R_0}{R_1}}\,. \tag{6.4}$$

Finally, the inverse Z-transform of $H(z)$ yields the spatial impulse response with respect to the node position in the resistive network:

$$h(n) = h(0) \cdot b^{|n|}\,, \qquad b = e^{-|a\cosh(1+R_1/2R_0)|} \tag{6.5}$$

where *h(0)* is a normalized coefficient [93]. Figure 6.12(a) plots the double-sided exponentially decaying IR in (6.5), whose decay constant is a function of R_1/R_0 ratio. The width of the impulse response is defined as the available spatial filter range to lower the variance of randomly distributed offsets through collective averaging.

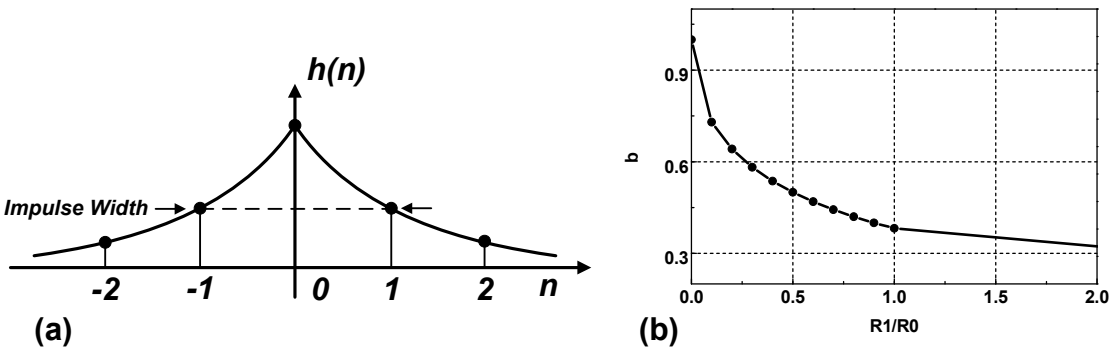

Figure 6.12: (a) Impulse response of the first-order resistive network; (b) Decay constant as a function of R_1/R_0 ratio.

Averaging network is optimum when it is designed as a matched filter, which means that the number of differential pairs in unclipped linear region is equal to the IR width [89], [91]. Figure 6.12(b) shows the relationship between *b* and R_1/R_0 ratio. Strong interaction between the neighbors can be achieved by choosing R_1/R_0 ratio small, thereby increasing the impulse width. Conceptually, smaller lateral resistor, R_1, introduces more interaction from the adjacent nodes to the node of interest, and this increase in interaction widens the spatial filter bandwidth.

6.2.5.2 Boundary Effect and Termination

Although the averaging network shows a positive effect for random offset reduction and SNR improvement, the amplifiers at the edge see non-linearity. Figure 6.13(a) shows the systematic offset near the edge of input range. The systematic offset is always the worst at the edge, and gradually decreases to zero in the middle of input range. For simplicity, only five amplifiers without random offset are considered. At the network boundaries, linearity degrades due to improper termination. This comes from the fact that the edge amplifier does not see the same number of neighbors contributing to its zero-crossing. Figure 6.13(b) demonstrates the first input zero-crossing at node *n(-2)* in the minimum of the input full-scale range. To the right of this zero-crossing, the amplifiers are still in the transition region up to node *n(-1)*, and the output currents are eventually clipped after node *n(0)*. To the left, one additional dummy amplifier ensures boundary continuity at the cost of input range overhead. The dummy stage guarantees the noise stimuli to the filter uniform across the input full-scale range. The number of the dummy amplifiers should be least equal to the minimum of the IR width or the number of active amplifiers around the zero-crossing.

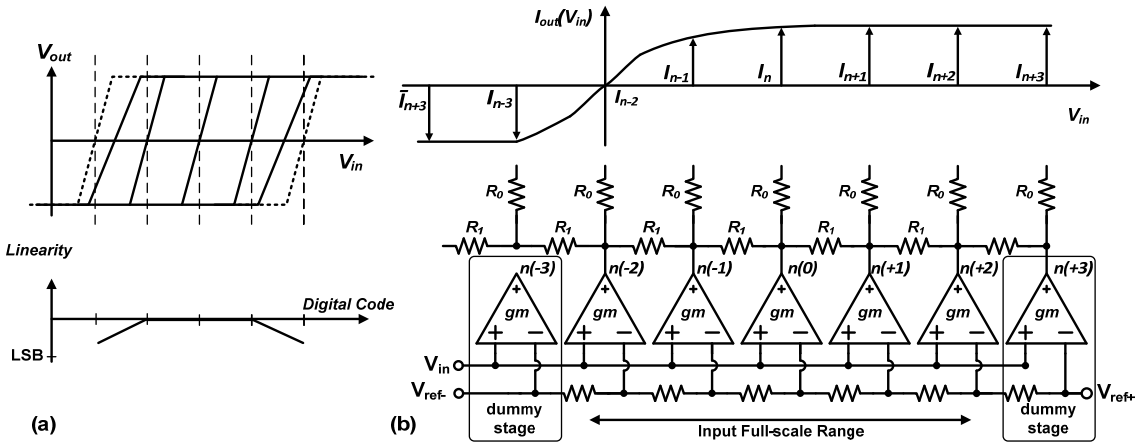

Figure 6.13: (a) Transfer characteristics of five amplifiers output; (b) Proper averaging network termination using dummy amplifiers.

Figure 6.13(b) also introduces a cross termination technique. The boundary of the system is terminated by coupling the lowest differential amplifier output with the inverted outputs from the highest amplifier in the array, resulting in a continuous loop of resistors. To the left of the dummy amplifier at node *n(-3)*, the output is connected to the opposite polarity of node *n(+3)* through a lateral resistor. Cross termination can be better understood by exploiting the odd symmetry between the positive and negative output nodes, as shown in Figure 6.14. Due to the odd symmetry, the zero-crossing is not affected by the averaging network, and the output currents of the positive amplifiers have exactly the same magnitude as the negative nodes. By connecting node *n(+2)* to negative node *n(-2)* with R_1, the network is no longer terminated abruptly at the boundary, and becomes circular with no termination. Therefore, the translational symmetry of the averaging network maintains the network's impulse response.

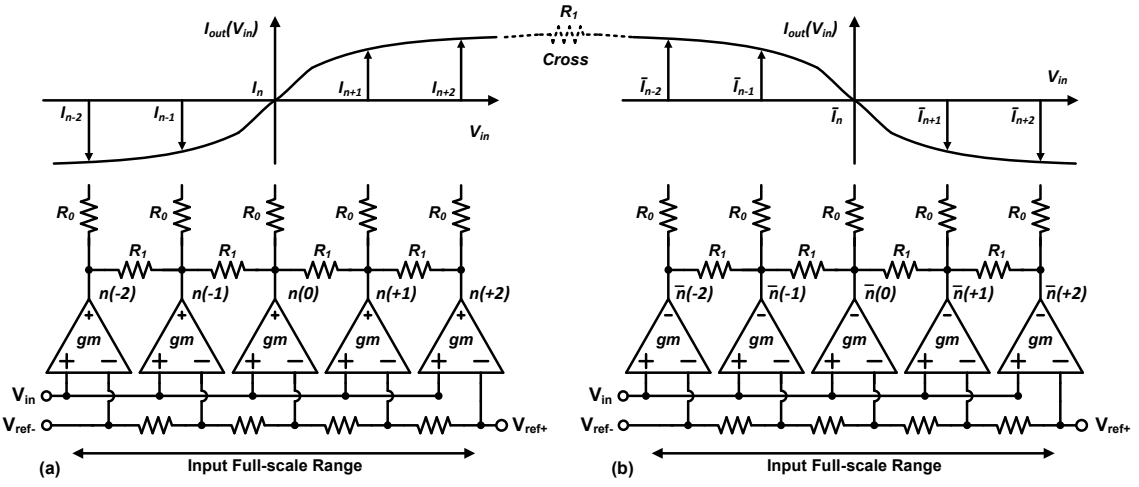

Figure 6.14: (a) Resistive network for positive output nodes; (b) Resistive network for negative output nodes.

Proper termination must be applied to restore the boundary linearity. There are three types of edge termination suitable for high-frequency applications: dummy termination, R_T termination, and cross termination. Figure 6.15(a) shows an array of nine amplifiers without averaging network. Dummy termination in Figure 6.15(b) is achieved by terminating the boundary with the same amplifiers, labeled edge. As the number of resolution increases, this method becomes inefficient because the additional dummy stages increase power consumption and input dynamic range. The second approach solves the issue of non-linearity by inserting only one additional stage and resizing the termination resistor at the boundary. In Figure 6.15(c), the termination resistor, R_T, at the two edges restores linearity when proper value is chosen. As derived in [94], the compensation resistor, R_T, is found to be $R_1 - R_0$. This seems attractive because only one extra stage is required on each end. The differential connection of cross termination is also shown in Figure 6.15(d).

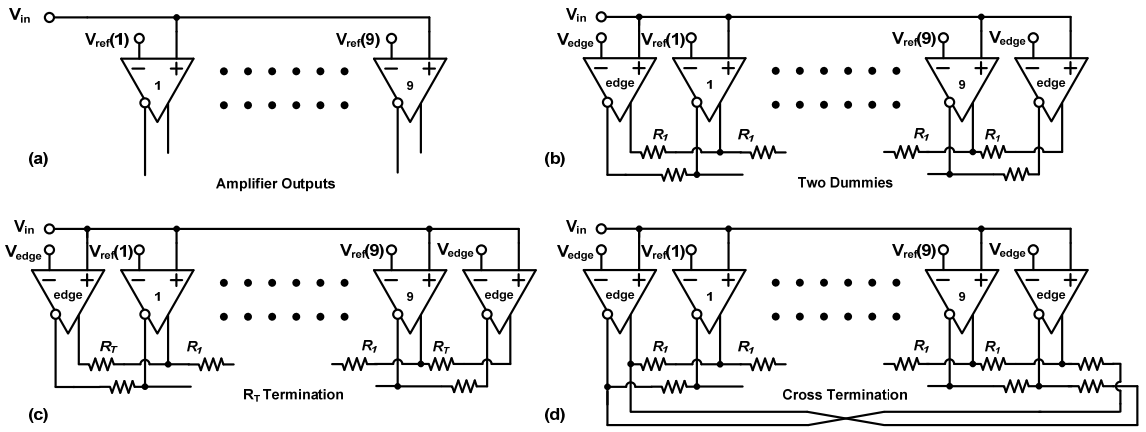

Figure 6.15: (a) Amplifier outputs without averaging; (b) Resistive averaging network with dummy termination; (c) R_T termination; (d) Cross termination.

Figure 6.16 shows the simulation results of amplifier outputs using different termination methods. For verification purpose, nine preamplifiers are chosen with an additional dummy stage on each end. The results indicate that all the nine zero-crossings of the amplifiers are well-restored using either termination method. However, in cross termination, the zero-crossing of the edge amplifiers shows better linearity, indicating 7% deviation from the ideal zero-crossing. On the other hand, the linearity using dummy termination and R_T termination is reduced by 22% and 30 %, respectively. This suggests that the boundary amplifier outputs using cross termination can be potentially used to extend the ADC resolution. Unlike cross termination, dummy and R_T terminations sacrifice the linearity of edge preamplifiers, thereby reducing the usable input range.

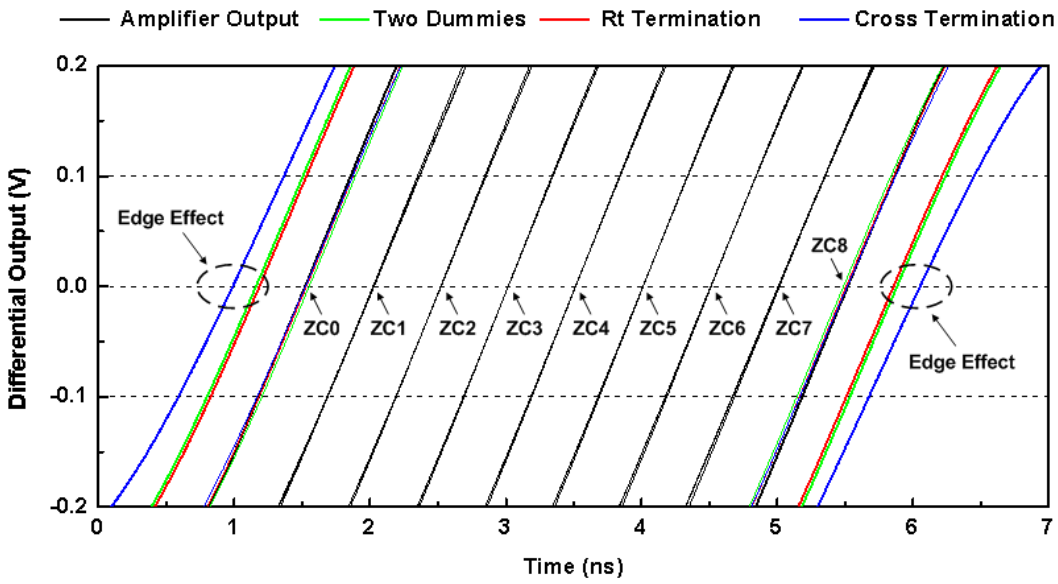

Figure 6.16: Simulation results of preamplifier outputs using various termination methods.

6.2.5.3 Speed Improvement

Not only does resistive averaging suppress both static and dynamic offsets due to the inherent CMOS process and circuit topologies, its improvement in bandwidth is discussed in this section. As explained earlier in (1.4), the input random offset voltage is inversely proportional to the square root of the transistor gate area. For reliable accuracy, the preamplifier transistor size related to the target ADC resolution is given by

$$\sigma_{VT} \approx \frac{A_{VT}}{\sqrt{W \times L}} \leq \frac{1}{4} LSB\,. \tag{6.6}$$

It has been shown that an optimum averaging network lowers random offset by up to 3x with a spatial impulse response of 18 zero-crossings wide [50], [91]. Since this work uses nine preamplifiers containing nine zero-crossings, an optimum averaging

network is said to lower random offset by up to 2x. With an optimum averaging network connected to the outputs of preamplifiers array, the same accuracy can be maintained using device size four times smaller than if no averaging were used. Considering a single-pole preamplifier output without averaging, its output bandwidth is estimated:

$$BW_{preamp} = \frac{1}{R_0 \cdot (C_{wire} + C_{junc} + C_{load})}, \tag{6.7}$$

where R_0 is the load resistor, C_{wire} is the parasitic capacitance due to wiring, C_{junc} is the gate-to-drain junction capacitance, and C_{load} is the input capacitance of the comparator. To achieve the same accuracy with averaging, four times smaller transistor size is chosen. For the same bias current and voltage gain, the load resistance must be twice larger since the transconductance and voltage gain are given by

$$gm = \sqrt{2 \cdot \mu_n \cdot C_{ox} \cdot \frac{W}{L} \cdot I_D}\ , \text{and } A_v = gm \cdot R_0, \tag{6.8}$$

where μ_n is the mobility of electrons, C_{ox} is the gate oxide capacitance per unit area, I_d is the static bias current, W is the device width, L is the device length, and R_0 is the load resistor. A single-pole preamplifier output with averaging is then derived:

$$BW_{preamp,avg} = \frac{1}{2R_0 \cdot (C_{wire}/4 + C_{junc}/4 + C_{load} + C_{netw})}, \tag{6.9}$$

where C_{netw} is the parasitic capacitance of the averaging network. Comparing (6.7) and (6.9), the speed improvement using averaging network is shown:

$$\frac{BW_{preamp}}{BW_{preamp,avg}} = \frac{2R_0 \cdot (C_{wire}/4 + C_{junc}/4 + C_{load} + C_{netw})}{R_0 \cdot (C_{wire} + C_{junc} + C_{load})}$$

$$= 2 \cdot [1 + \frac{C_{netw}}{C_{wire} + C_{junc} + C_{load}} - \frac{3}{4} \cdot \frac{C_{wire} + C_{junc}}{C_{wire} + C_{junc} + C_{load}}] \approx \frac{1}{2}. \qquad (6.10)$$

The second term in (6.10) is much less than one, while the third term is close to one. Therefore, the use of averaging raises the preamplifier bandwidth by almost double.

6.2.6 Random Offset Reduction Analysis

One of the ways to reduce offset voltage is to lower the value of averaging resistor R_1. Beyond certain extent, this approach becomes ineffective as gain starts to roll off. Figure 6.17 shows the simulation results of amplification reduction and offset reduction in the middle array as a function of R_1 for preamplifier and comparator stages, respectively. For each R_1/R_0 ratio, the static offset voltage is collected from 1000 Monte Carlo trials, and the corresponding standard deviation (σ) is calculated in mV. The offset reduction ratio is measured as the ratio of the input-referred offset in rms value before averaging to that after applying averaging. The voltage gain of the preamplifier, normalized to the gain at infinite averaging R_1, is also obtained for various R_1/R_0 ratios. Interestingly, when the R_1/R_0 ratio is small, the amplification gain attenuates at a rate faster than the offset voltage. As discussed before, the gain of the preamplifier must be high enough for the required metastability error rate. Without sacrificing the voltage gain of the preamplifier stage, the R_1/R_0 ratio is chosen to be five, which provides an offset

reduction ratio of 0.76. Since the latch following comparator output usually suffers the most due to both static and dynamic mismatches, the R_1/R_0 ratio at the first comparator stage output is chosen to be 2.5 to suppress the random offset by a factor of 0.67.

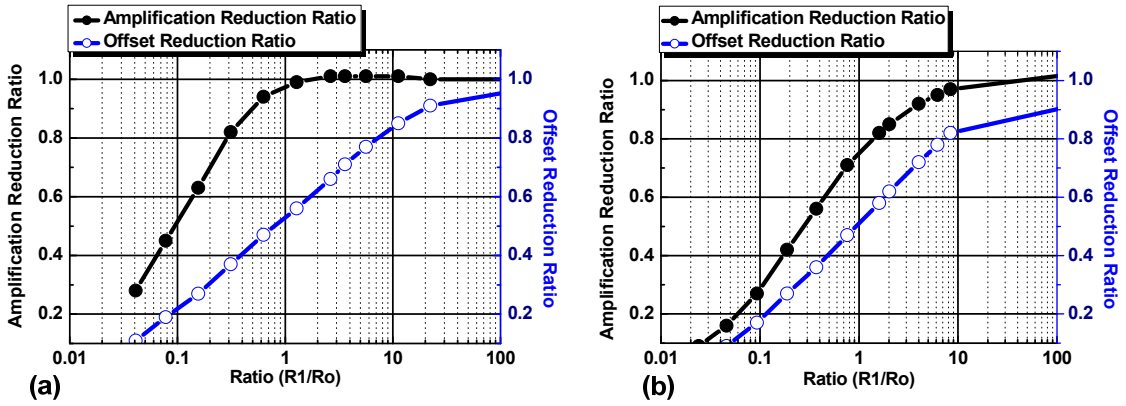

Figure 6.17: Amplification and offset reduction as a ratio of R_1/R_0 for (a) preamplifier stage and (b) comparator stage, respectively.

A typical rule of thumb for ADC design is that the 3σ value of comparator offset should be less than 0.5 LSB, so the comparator offset guarantees a standard deviation of 0.2 LSB or better. Since the full-scale differential input level of the high-performance 3-bit ADC is 400 mVpp, a differential LSB size is 50 mV. With a 0.2 LSB target, the input-referred offset voltage should have a standard deviation less than 10 mV. In order to meet this offset requirement, the design of preamplifier, first comparator and cross termination averaging is analyzed. Although the voltage gain of preamplifier and comparator stage reduces the input-referred offset of the regenerative latch, the differential input pairs create additional offset. Reducing the offset of the preamplifier through device sizing is

power and speed inefficient approach. Therefore, resistive averaging network is applied to reduce offset in the analog amplifiers.

The analysis begins with a detailed diagram shown in Figure 6.18. Given the schematic, the input-referred offset with averaging network is given by

$$V_{os,in} = \xi_{pre} \cdot V_{os,pre} + \xi_{cmp} \cdot \frac{V_{os,cmp}}{A_{v,pre}} + \frac{V_{os,latch}}{A_{v,pre} \cdot A_{v,cmp}} \tag{6.11}$$

where $V_{os,pre}$, $A_{v,pre}$, and ξ_{pre} are the input-referred offset, voltage gain, and offset reduction ratio due to averaging of the preamplifier, respectively, $V_{os,cmp}$, $A_{v,cmp}$, and ξ_{cmp} are the input-referred offset, voltage gain, and offset reduction ratio due to averaging of the comparator, respectively, and $V_{os,latch}$ is the input-referred offset of the latch. The offset reduction ratio, ξ, is a function of the averaging resistor and the amplifier output resistance, and is also determined by the number of linear active amplifier stages.

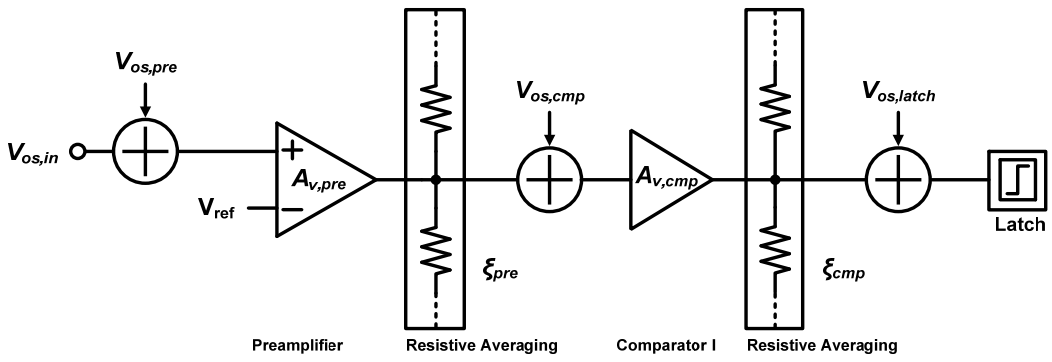

Figure 6.18: Offset reduction analysis using a preamplifier-based comparator with averaging network.

Table 6.5 lists the voltage gain, 3 dB bandwidth, input-referred offset, offset reduction ratio for preamplifier and comparator stages. The input-referred offset rms value of the preamplifier ($\sigma_{os,pre}$) is calculated using (1.4), where the transistor threshold mismatch coefficient is obtained from Figure 1.2, and device width and length are obtained in Figure 6.6. The input-referred rms offsets of comparator and latch ($\sigma_{os,cmp}$ and $\sigma_{os,latch}$) are collected from 1000 Monte Carlo trials.

Since each of the input-referred offsets has an offset that is uncorrelated to one another, their variances add. Using the parameters from Table 6.5, (6.11) can be expressed as

$$\sigma_{os,in} = \sqrt{\xi_{pre}^2 \cdot \sigma_{os,pre}^2 + \xi_{cmp}^2 \cdot \frac{\sigma_{os,cmp}^2}{A_{v,pre}^2} + \frac{\sigma_{os,latch}^2}{A_{v,pre}^2 \cdot A_{v,cmp}^2}}$$

$$= \sqrt{\xi_{pre}^2 \cdot \frac{A_{VT,pre}^2}{W \times L} + \xi_{cmp}^2 \cdot \frac{\sigma_{os,cmp}^2}{A_{v,pre}^2} + \frac{\sigma_{os,latch}^2}{A_{v,pre}^2 \cdot A_{v,cmp}^2}} \tag{6.12}$$

The width and length of the preamplifier's input transistor are chosen to be 5 µm and 100 nm for high bandwidth. The calculated offset voltage using the preamplifier-based comparator and resistive averaging network is 8.33 mV based on the simulation results, which is less than the targeted 10 mV offset.

Table 6.5: Voltage gain, 3 dB bandwidth, input-referred offset voltage, and offset reduction ratio for each stage.

	Voltage gain (A_v)	Input-referred offset (σ_{os}) in mV without averaging	Offset reduction ratio due to averaging (ξ)	3 dB bandwidth in GHz
Preamplifier	2.822	4	0.76	6.7
Comparator	3.19	29.92	0.67	5
Latch	—	23.93	—	—

6.2.7 Digital Back-End

The reset switch employed in the preamplifier and comparator suppresses the bubble errors caused by inadequate overdrive recovery. The output of the second comparator passes through another regenerative SR latch stage, followed by a high-speed logic gate-based encoder. Logic gate-based encoding is also chosen because it is more tolerant to an undefined comparator output [95], where each comparator output is used only once. The intermediate gray encoding reduces the probability of metastability error by ensuring that the output from any comparator affects only one bit in the output code, as shown in (6.13)-(6.15), hence improving the BER of the comparators [61], [94], [95]. To further reduce the probability of an unsettled thermometer output, DFFs are inserted between the logic stages as well as the input and output interfaces. Using the thermometer encoding, gray encoding can be expressed as

$$G[0] = T[0]\overline{T[2]} + T[4]\overline{T[6]}, \tag{6.13}$$

$$G[1] = T[1]\overline{T[5]}, \tag{6.14}$$

and

$$G[2] = T[3], \tag{6.15}$$

where *T[n]* is the *nth* thermometer code output, and n = 0, 1, ..., 6. The simplified schematic is shown in Figure 6.19. According to simulation, the fully-pipelined encoder using standard-cell ASIC consumes 1.5 mW at 3.456 GHz sampling rate.

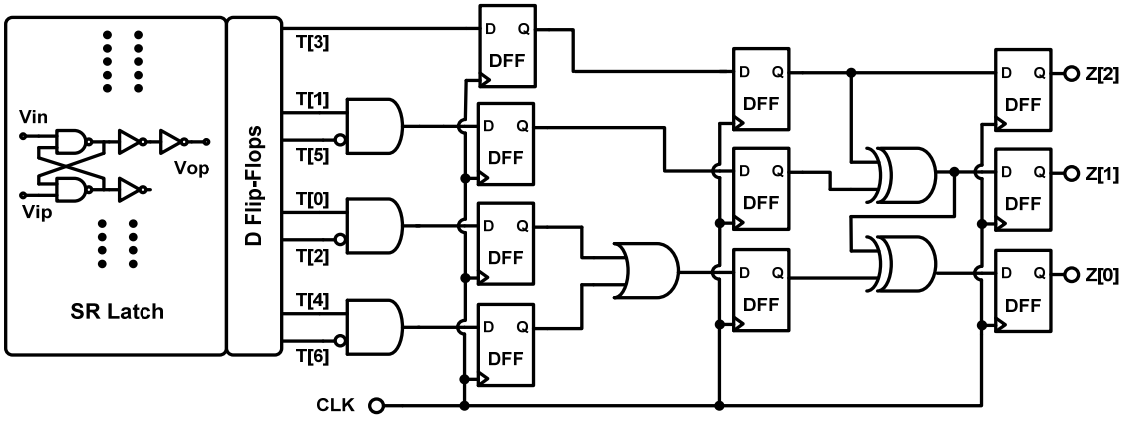

Figure 6.19: Schematic of the digital back-end.

6.2.8 Performance Summary

The high-performance 3-bit flash ADC layout is shown in Figure 6.20(a), which occupies an active area of 225 μm x 190 μm. Since the layout is fully symmetric, the differential clock signal can be evenly distributed to the individual ADC channel, avoiding any unbalanced clock edge arrivals. According to the parasitic layout extraction, clock rise and fall time increases from 17 ps to 32 ps. This is about 150 fF parasitic

capacitance due to metal interconnect. Figure 6.20(b) shows the power consumption breakdown of each component at 6.912 GS/s. Clearly, the most power-hungry building block is the preamplifier mainly for maximum linearity, which occupies 35.17 % of the overall power budget.

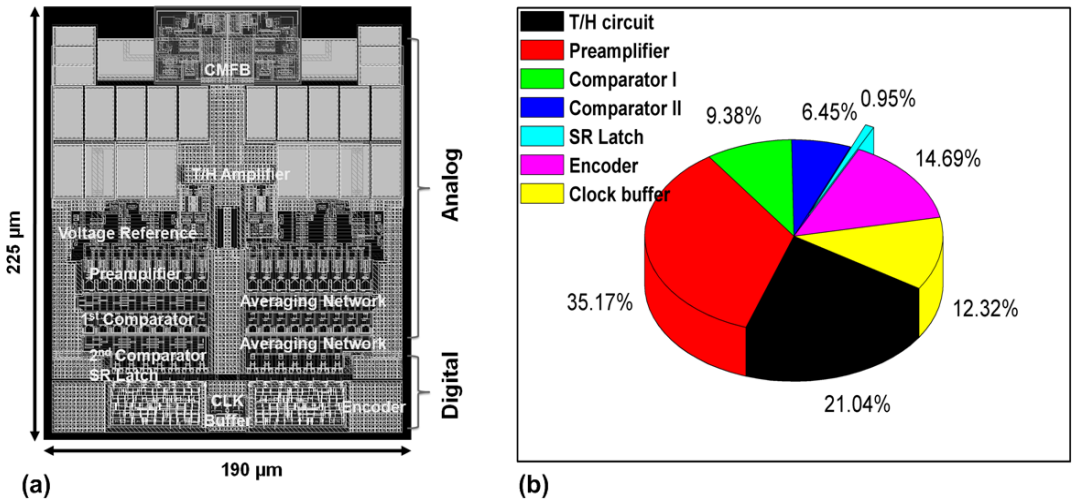

Figure 6.20: (a) Fully-symmetric ADC layout; (b) Power consumption breakdown.

The parasitic extracted schematics have been analyzed to obtain both static and dynamic performances using histogram test or known as the code density test [79]. To exacerbate the simulation environment, a 200 pH inductor is added in series with the supply line to emulate supply noises. Figure 6.21 shows the linearity performance of the ADC. The averaging network strongly averages out the transistor random offset by correlating to its adjacent stages in the linear range. Now each preamplifier and comparator stages see a much bigger device size. As a result, the worst DNL and INL

based on code density test are both less than 1 LSB for an input 1 MHz sine wave at 4 GS/s.

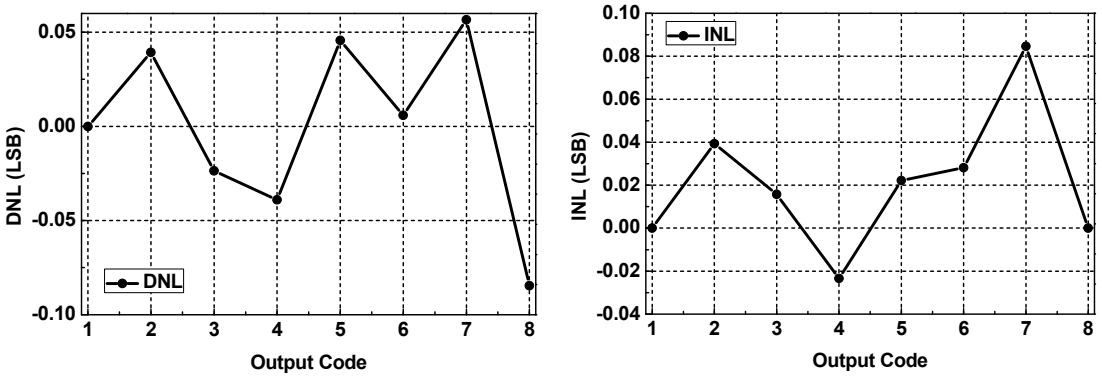

Figure 6.21: DNL and INL for f_{in} = 1 MHz at 4 GS/s sampling rate.

The dynamic performance of the ADC is summarized in Figure 6.22. Single-channel ADC performance is analyzed at 4 GS/s to compare with the measurement results obtained from the 3 GS/s low-power (3 mW) ADC design in Chapter 5. The goal is to differentiate the performance improvement using this high-performance ADC, compared with the low-power ADC in Chapter 5. Four test cases are considered here: ideal simulation at 4 GS/s, parasitic extraction (PEX) at default power, PEX at maximum power, and Monte Carlo simulation at 4 GS/s. In any test cases, the dynamic performance shows superior improvement compared to the low-power ADC. When the maximum power is selected, SFDR and SNDR improve at least 4 dB and 3 dB, respectively, for an input frequency up to 1.485 GHz. Detailed performance summary is shown in Table 6.6.

The total power consumption of the two-channel time-interleaved ADC is measured to be 19 mW at 6.912 GS/s.

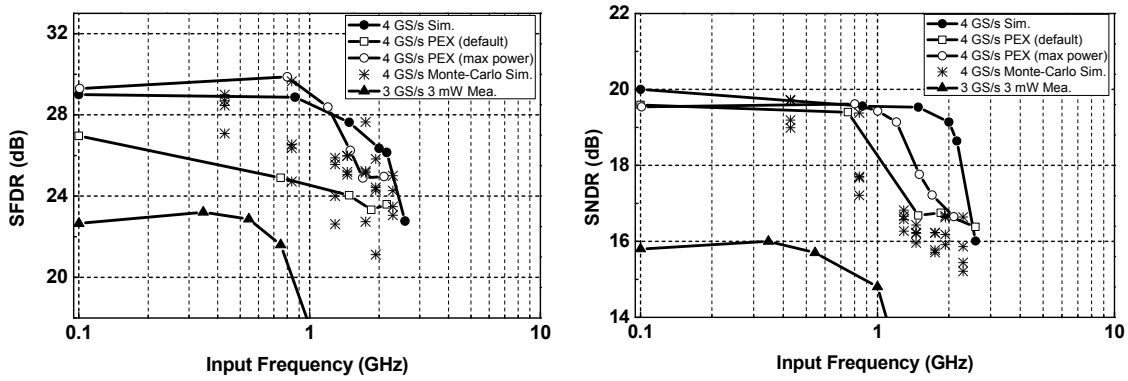

Figure 6.22: SFDR and SNDR of the single-channel ADC at 4 GS/s.

Table 6.6: Performance summary of the single-channel 4 GS/s ADC.

Specification	Parameter		Unit
Supply voltage	1		V
Input range	400		mVpp
Sampling rate	4		GS/s
ERBW	1.75		GHz
Power consumption	10	11.5	mW
SFDR	29.3 @ fin = 100 MHz	24.8 @ fin = 2 GHz	dB
SNDR	19.5 @ fin = 100 MHz	16.5 @ fin = 2 GHz	dB
ENOB	2.95 @ fin = 100 MHz	2.45 @ fin = 2 GHz	bit
FOM	0.32	0.526	pJ
DNL/INL	< 0.1		LSB
Active area	0.04275		mm^2

6.3 Dual-Mode Multi-Gigabit Mixed-Signal Demodulator

Figure 6.23 shows the block diagram of the dual-mode mixed-signal demodulator. The IF analog front-end consists of the same components, as discussed in Chapter 5. In order to achieve an ultra-high-speed baseband sampling rate, each channel utilizes two identical high-performance 3-bit flash ADCs with resistive averaging network. This effectively enables a sampling rate of 6.912 GS/s per channel, which is the Nyquist requirement to recover a data capacity of 3.456 Gbps. Following the ADC is the mode select block. This block is designed to turn off one channel of the time-interleaved ADC completely in case when the input data rate is lower than 1.728 Gbps. As a result, the power consumption of the high-performance ADC can be decreased from 19 mW to 11 mW, and the sampling rate becomes 3.456 GS/s per baseband channel. The high-speed baseband DSPs features both non-coherent ASK demodulation and coherent BPSK demodulation. To realize gigahertz digital signal processing using standard-cell ASIC design flow, both the ADCs and the digital demodulator employee two-channel time-interleaved topology to meet the stringent timing specifications in 90 nm digital CMOS process.

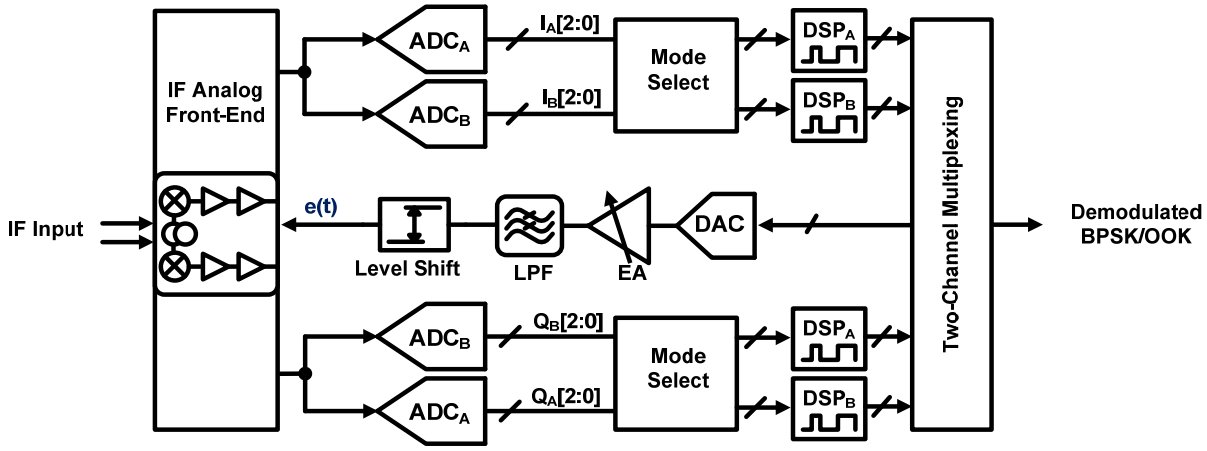

Figure 6.23: Block diagram of the dual-mode multi-gigabit mixed-signal demodulator.

6.3.1 Non-Coherent ASK Demodulator

The concept of the multi-gigabit digital ASK demodulator utilizes the inherent characteristics of an IF quadrature down-converter, as shown in Figure 6.24. Assuming the IF ASK modulated signal after the IF VGAs is given by

$$R_{ASK,IF}(t) = A \cdot \cos(\omega_c \cdot t), \tag{6.16}$$

where A is the amplitude, and ω_c is the IF carrier frequency. The down-converted low-passed baseband I and Q signals can be shown to be:

$$I_{channel}(t) = A' \cdot \cos((\omega_c - \omega_{vco}) \cdot t + \phi) \text{ and } Q_{channel}(t) = A' \cdot \sin((\omega_c - \omega_{vco}) \cdot t + \phi), \tag{6.17}$$

where A' is the amplifier after baseband AGCs, and ω_{vco} is the output frequency of the IF QVCO with a constant phase error of ϕ. Therefore the baseband signals experience a constant 90 degrees phase difference between I and Q channels.

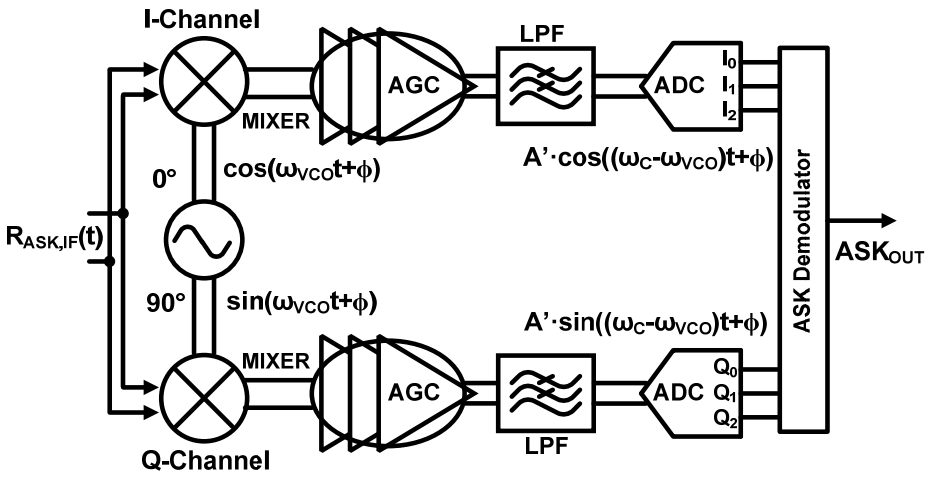

Figure 6.24: Block diagram of the IF front-end with non-coherent ASK demodulator.

The original binary data stream and the ASK modulated signal are shown in Figure 6.25(a) and Figure 6.25(b), respectively. Figure 6.25(c) and Figure 6.25(d) illustrate the waveforms of the non-coherently detected baseband signals. To recover an ASK modulated signal, $I^2 + Q^2$ amplitude detection is usually performed in analog domain [34], [38], [39].

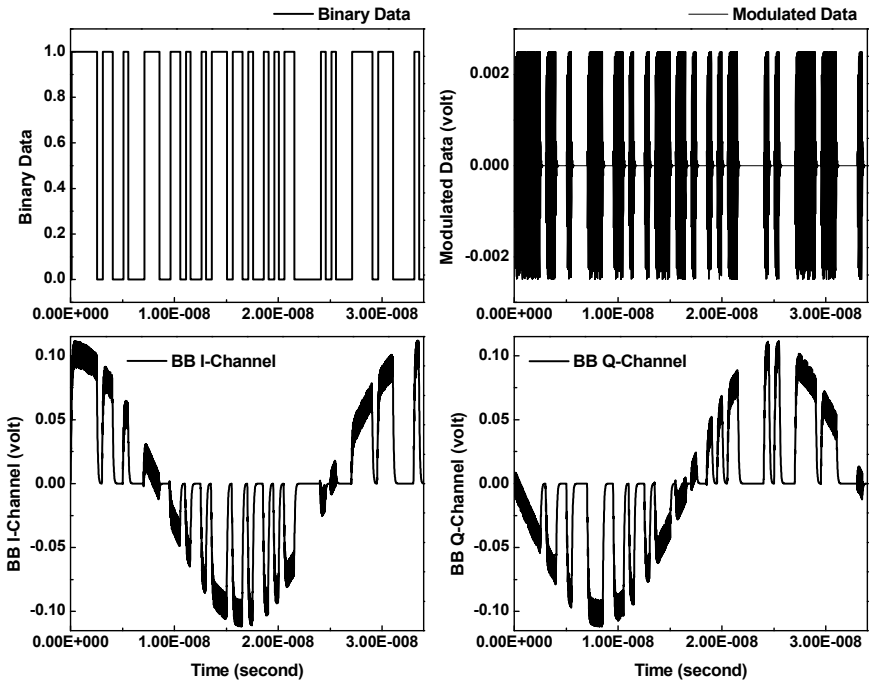

Figure 6.25: (a) Binary data stream; (b) ASK modulated IF signal; Down-converted baseband (c) I channel and (d) Q channel signals with 30 MHz frequency offset.

The proposed digital ASK demodulator requires oversampling the ADCs at a constant frequency of 6.912 GHz to avoid anti-aliasing. To decide whether the current data polarity is a logic zero or one, amplitude detection is applied by performing XNOR operation between the two MSBs in each channel and sums the result with an OR operation (refer to Figure 6.26). This is equivalent of doing squaring function in analog domain. The demodulated ASK signal can be expressed as

$$ASK_{out} = \overline{I[2] \oplus I[1]} \cup \overline{Q[2] \oplus Q[1]}, \tag{6.18}$$

where *I[2]* and *Q[2]* are the MSB of I channel and Q channel, respectively. Since the phase of baseband channels are off by a constant 90 degrees, when the amplitude of I

channel is at zero, the amplitude of Q channel should be at its maximum or minimum. By reading these two channels simultaneously, the original binary data stream can always be recovered. As long as the envelope amplitude crossing point between the baseband I/Q waveforms is large than half of the ADC full-scale dynamic range (0.707 * V_{in} > 0.5 * V_{FS_ADC}), the proposed digital ASK demodulator operates properly. In other words, the minimum sensitivity of the ASK demodulator is 0.707 * V_{FS_ADC}. In the DSP operation, the baseband power level is always set to the full-scale range of the ADCs, which is -10 dBm in this work.

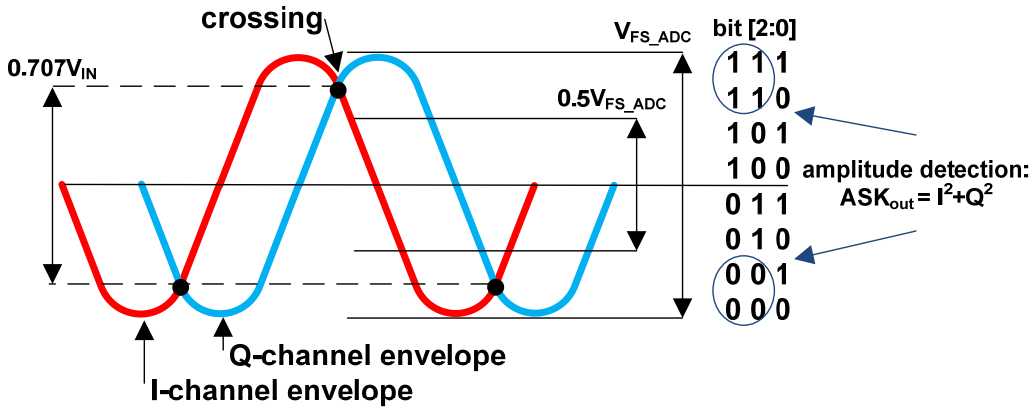

Figure 6.26: Concept of recovering an ASK modulated signal.

6.3.2 Coherent BPSK Demodulator

The concept of the coherent BPSK demodulator based on modified Costa loop theory has been discussed in Chapter 5 and it has been measured and validated at a IF frequency of 13 GHz. This chapter demonstrates its feasibility by integrating with 60

GHz receiver front-end and optimizing the analog design of error amplifier and QVCO level shifter to target an error-free transmission at 3.5 Gbps.

6.3.2.1 Mode Select

Unlike non-coherent ASK demodulation, the coherent BPSK demodulator does not require oversampling at 6.912 GS/s. Therefore, the overall power consumption of the mixed-signal demodulator can be lowered by making the ADC in Nyquist mode, as shown in Figure 6.27 and Table 6.7. Enabling the Nyquist mode decreases the power consumption by 40 %. For example, there are two ways to enable a sampling rate of 3.456 GS/s. In interleaved mode, the baseband frequency synthesizer only has to provide a clock frequency of 1.728 GHz, where as in Nyquist mode, one ADC core is turned off, requiring a baseband frequency of 3.456 GHz. The trade-off between the interleaved mode and Nyquist modes is receiver minimum sensitivity.

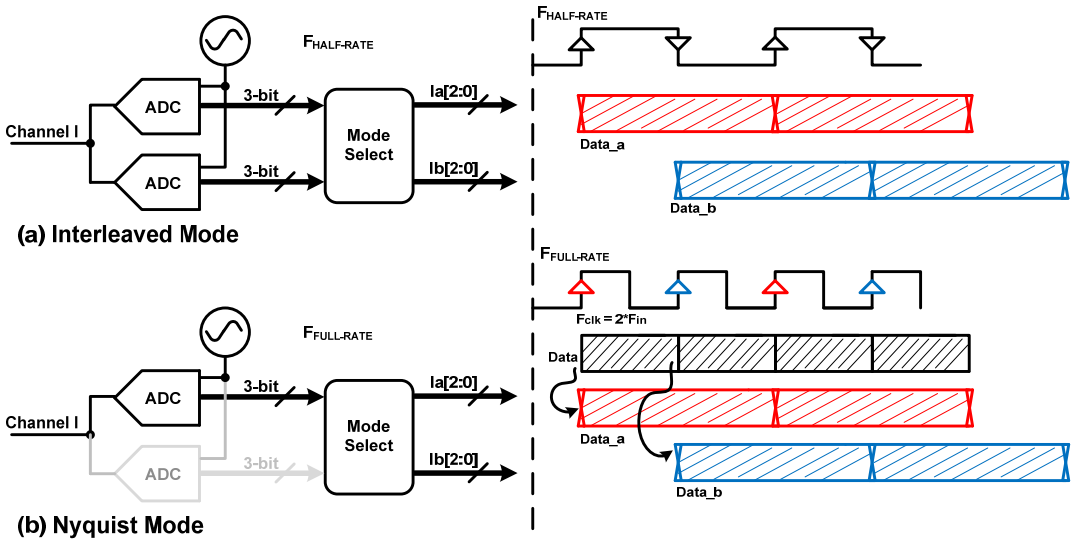

Figure 6.27: Functional diagram of ADC operating modes.

Table 6.7: ADC measured power consumption breakdown in different modes.

Specification	Parameter		Unit
Mode	Interleaved	Nyquist	—
Clock input	1.728		GHz
Power consumption	16.5	9	mW
Effective sampling rate	3.456	1.728	GS/s
Clock input	3.456		GHz
Power consumption	19	11	mW
Effective sampling rate	6.912	3.456	GS/s

6.3.2.2 Error Amplifier

The schematic of the error amplifier is shown in Figure 6.28. Similar to Figure 5.29, it consists of common-drain stage and common-source stages with degeneration and diode load to attenuate input signal. This error amplifier is designed to tolerate output DC voltage variation. The output DC voltage is directly coupled to the *Vtune* of the QVCO,

which exhibits a high K_{VCO} gain of 2.9 GHz/V. Depending on the error signal amplitude, variable gain is achieved by selecting *out1* or *out2* using *ctrl* control.

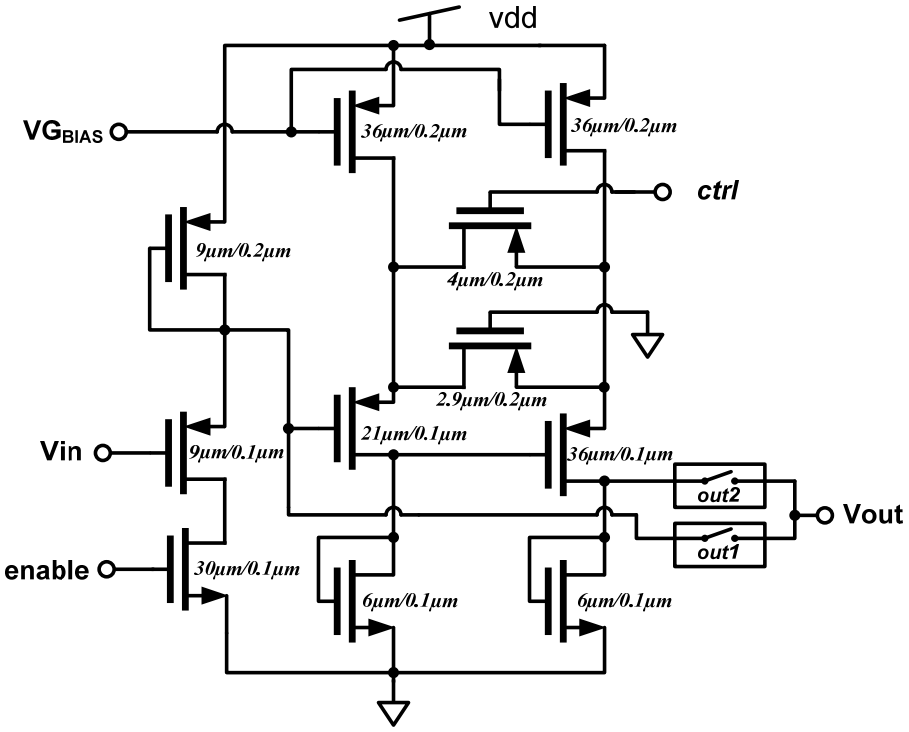

Figure 6.28: Schematic of the error amplifier.

The output bias voltage and voltage gain are verified by sweeping the input from 60 mV to 200 mV, as shown in Figure 6.29. The 3 dB bandwidth is relatively flat because the gain variation is nearly none. The *gm* from the diode load cancels out the nonlinearity of the input transistor. Therefore, linearity is maintained and transistor mismatch is minimized without using poly resistors. Its performance summary is shown in Table 6.8.

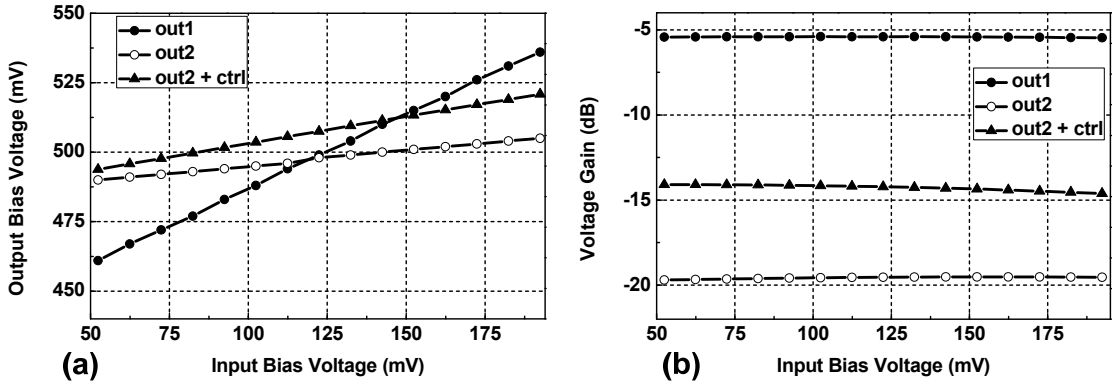

Figure 6.29: Output DC voltage variation versus input voltage sweep; (b) Voltage gain variation versus input voltage sweep.

Table 6.8: Performance summary of the error amplifier.

Specification	Parameter			Unit
Supply voltage	1			V
Current consumption	1.5			mA
Input bias voltage	125			mV
Control bit	*out1*	*out2*	*out2 + ctrl*	—
Voltage gain	-5.4	-19.5	-14.2	dB
3 dB bandwidth	3.3	2.5	2.87	GHz
Output bias voltage	499	498	507	mV

6.3.2.3 QVCO Level Shifter

The QVCO level shifter acts as a switch between the IF PLL and mixed-signal demodulator. Prior to coherent BPSK demodulation, the PLL can be first enabled to lock the free-running QVCO. By remembering the settled voltage from PLL, V_{BIAS} is fixed to the remembered voltage and the output of the error amplifier feeds directly to V_{in}, as shown in Figure 6.30. Detailed performance summary is listed in Table 6.9.

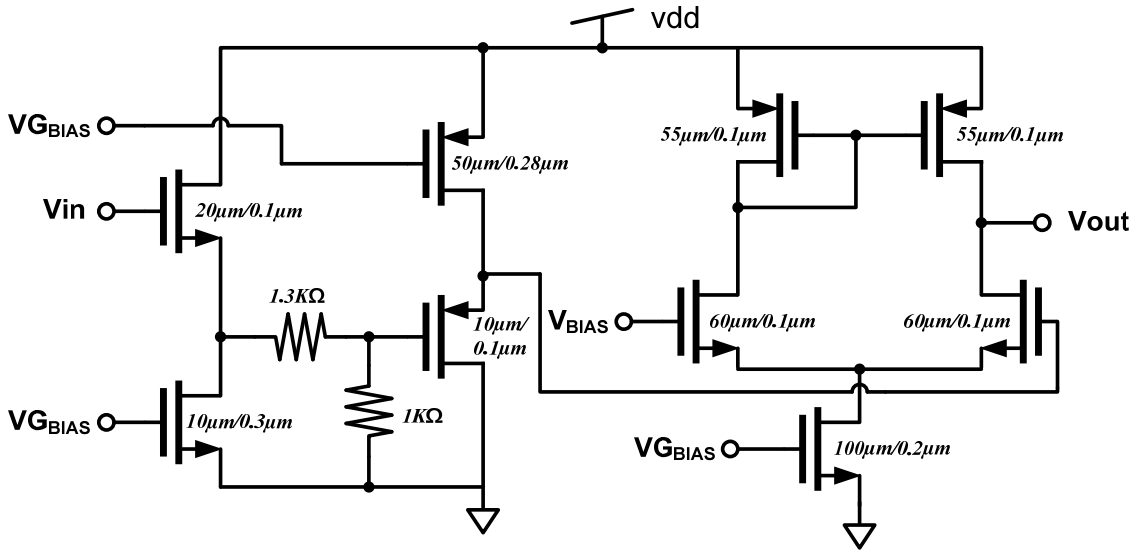

Figure 6.30: Schematic of the QVCO level shifter.

Table 6.9: Performance summary of the QVCO level shifter.

Specification	Parameter	Unit
Supply voltage	1	V
Current consumption	3.5	mA
Voltage gain	0.619	dB
3 dB bandwidth	1.12	GHz
Input bias voltage	500	mV
Output bias voltage	508.5	mV

6.4 Measurement Setup

Figure 6.31 shows the measurement setup of the dual-mode mixed-signal 60 GHz receiver. In this measurement, an off-the-shelf 2x subharmonic mixer is first used as an up-converter. PRBS data input and 31.32 GHz local oscillator are chosen to produce an ASK modulated carrier at 62.64 GHz. While testing the DSP speed performance, both the RF and IF AGCs are set to provide a constant baseband power level of -10 dBm to the

ADC input. This ensures that the digital ASK demodulator has a sufficient baseband amplitude swing of at least 0.707 * V_{FS_ADC}, as discussed in the previous section. The coherent BPSK demodulator is also characterized and measured in similar fashions. The fabricated multi-mode mixed-signal receiver is controlled by the serial peripheral interface (SPI) consisting of four-bit bus: serial clock (SCLK), master output slave input (MOSI), slave select (SS), and reset (RST).

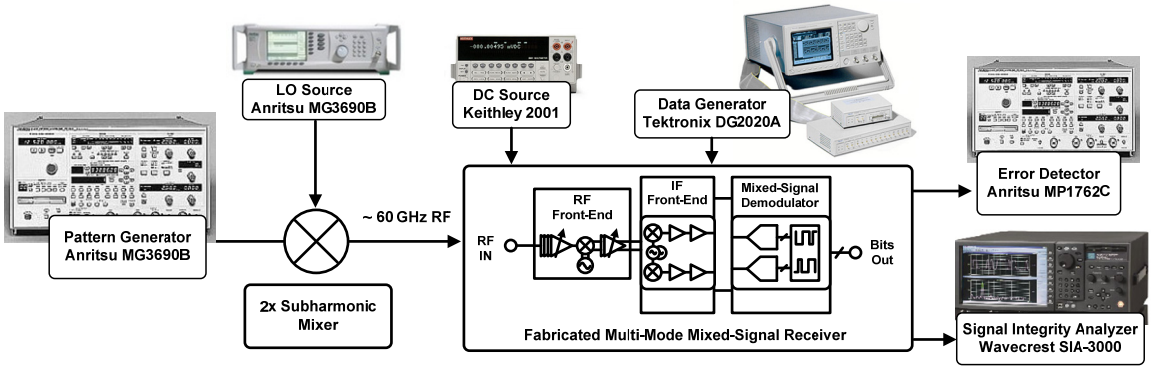

Figure 6.31: Measurement setup of the dual mode mixed-signal receiver.

6.5 Measurement Results

The multi-mode mixed-signal ASK/BPSK demodulator is fabricated using a standard 90 nm digital 1P7M CMOS process and occupies an area of 1.25 mm x 2. 5 mm (including all I/O pads), as shown in Figure 6.32.

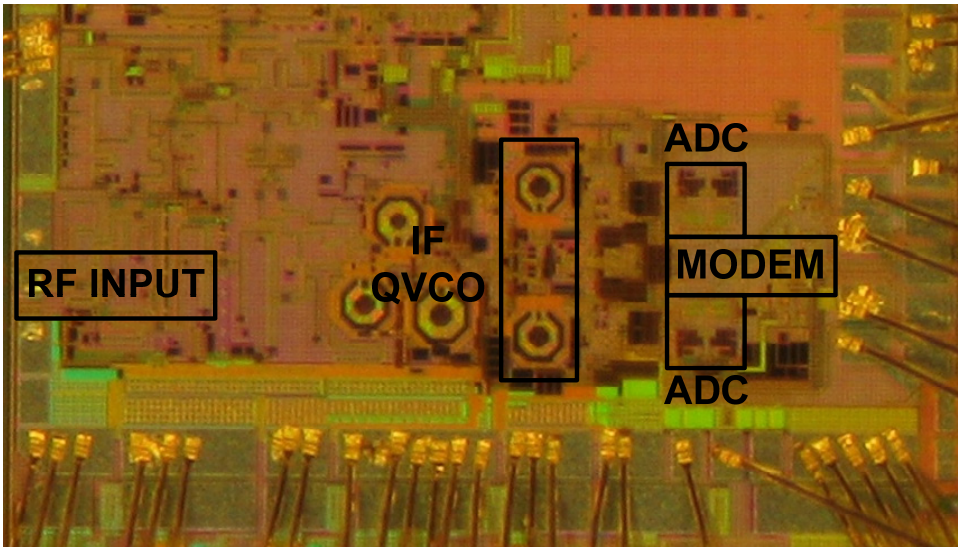

Figure 6.32: Microphotograph of the multi-mode mixed-signal demodulator.

6.5.1 Non-Coherent ASK Results

At the probing pad, the RF input power level is characterized to be -48.5 dBm. Figure 6.33(a) and Figure 6.33(b) show the demodulated eye-diagrams of the non-coherent ASK demodulator at 864 Mbps and 1.485 Gbps, respectively. With a constant ADC sampling rate of 6.912 GS/s and a RF input power level of -48.5 dBm (as depicted in Figure 6.34(a)), the measured ASK demodulator achieves a BER of 1.5E-08, 7E-08, and 9E-07 at 864 Mbps, 1.485 Gbps, and 1.728 Gbps, respectively, for 2^{31}-1 PRBS data rates. Figure 6.34 (b) shows the minimum sensitivity of the receiver at different data rates. The lowest minimum sensitivity occurs at a RF input power level of -51 dBm.

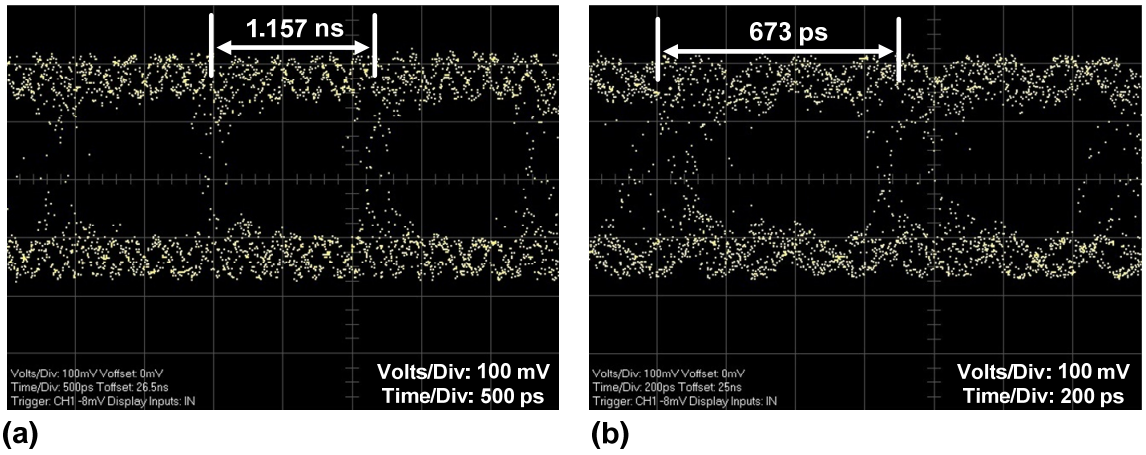

Figure 6.33: Demodulated eye-diagrams of the non-coherent ASK demodulator at a data rate of (a) 864 Mbps and (b) 1.485 Gbps, respectively.

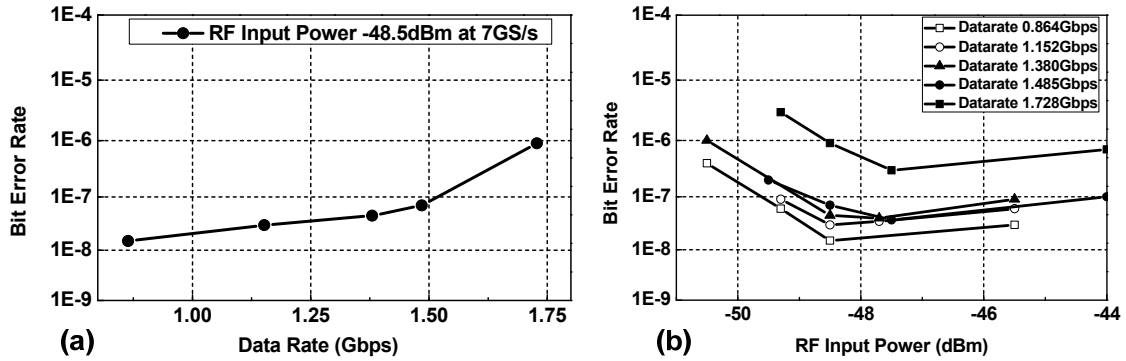

Figure 6.34: (a) Data rates versus BER at a RF input power of -48.5 dBm; (b) RF input power levels versus BER at various data rates.

The BERs obtained in this work are the raw demodulated data without additional digital processing nor error correction circuitries. Error free transmission is not obtained because the non-coherent detector requires a bit synchronizer to ensure that every sampling falls within each symbol period prior to digital processing. However, oversampling by at least a factor of four at 6.912 GS/s, a decent BER of is observed.

6.5.2 Coherent BPSK Results

The performance of the coherent BPSK demodulator is first characterized using single-channel Nyquist ADC at a sampling rate of 1.728 GS/s and 3.456 GS/s, respectively. The demodulator is operating in low-power mode. Figure 6.35(a) shows the measured BER at various RF input power levels at a sampling rate of 1.728 GS/s. The demodulator achieves error-free transmission up to 2.5 Gbps at a RF input power level of -44 dBm. At 864 Mbps, its receiver sensitivity is -52 dBm. The same test is performed by operating the baseband clock at 3.456 GS/s. Figure 6.35(b) shows the improved receiver sensitivity of -54.5 dBm at 864 Mbps. In additional, an error-free transmission for 3.456 Gbps data rate is observed at -36 dBm. By enabling the mode select block, a fully-integrated two-channel time-interleaved ADC in the mixed-signal demodulator is also characterized at a sampling rate of 3.456 GS/s and 6.912 GS/s, respectively (refer to Figure 6.36). A minimum sensitivity for error-free transmission is observed to be -54.5 dBm, and error-free transmission at 3.456 Gbps is maintained. The synchronization range and minimum sensitivity both improve with higher sampling rate; hence interleaved mode is preferred at 6.912 GS/s. It is also verified that operating a single-channel ADC at 3.456 GS/s does not degrade the system. Narrower loop bandwidth is desired for coherent BPSK demodulation to maintain stable loop response because the high-performance ADC takes eleven conversion cycles.

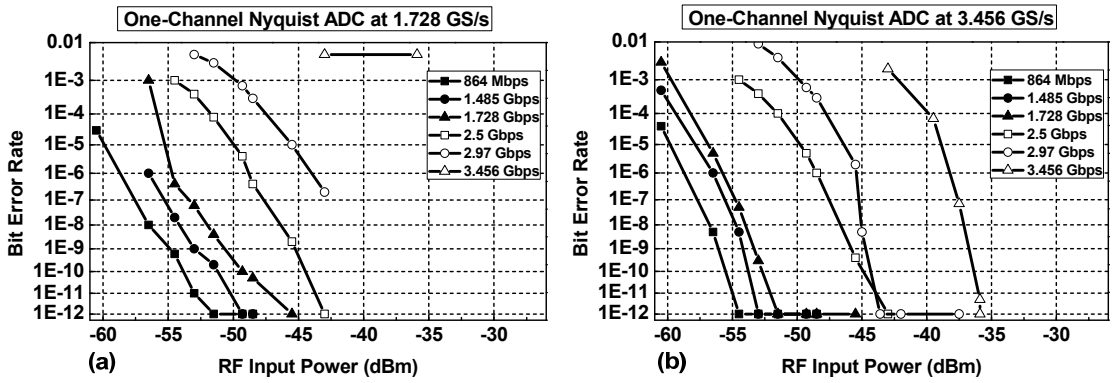

Figure 6.35: Measured BER at various RF input power levels using one-channel Nyquist ADC at (a) 1.728 GS/s and (b) 3.456 GS/s, respectively.

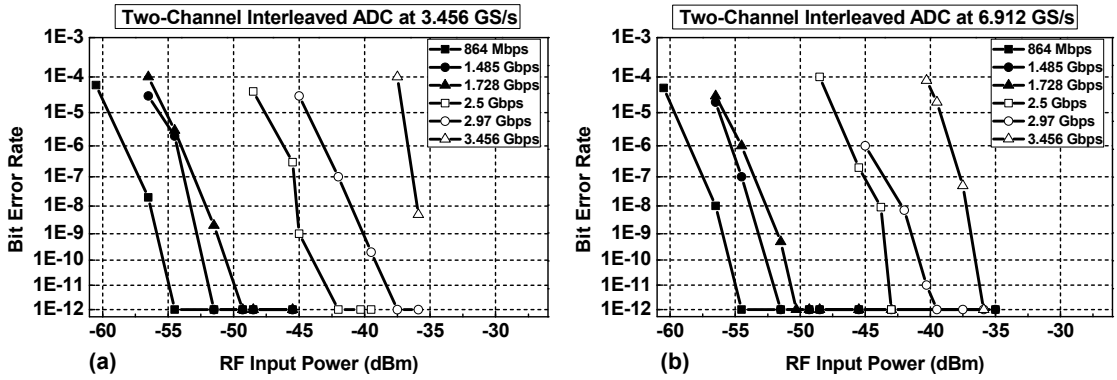

Figure 6.36: Measured BER at various RF input power levels using two-channel time-interleaved ADC at (a) 3.456 GS/s and (b) 6.912 GS/s, respectively.

Figure 6.37(a) captures the demodulated eye-diagram at 2.5 Gbps and Figure 6.37(b) shows the demodulated eye-diagram at 3.456 Gbps. Compared to the ones captured in Figure 5.35, these eye-diagrams exhibit significantly lower noise on the supply lines. Overall, the maximum data rate achieves better than 3.456 Gbps. The current limitation to the maximum achievable data rate is the analog bandwidth of the

baseband VGAs as well as the maximum operating frequency of the baseband frequency synthesizer.

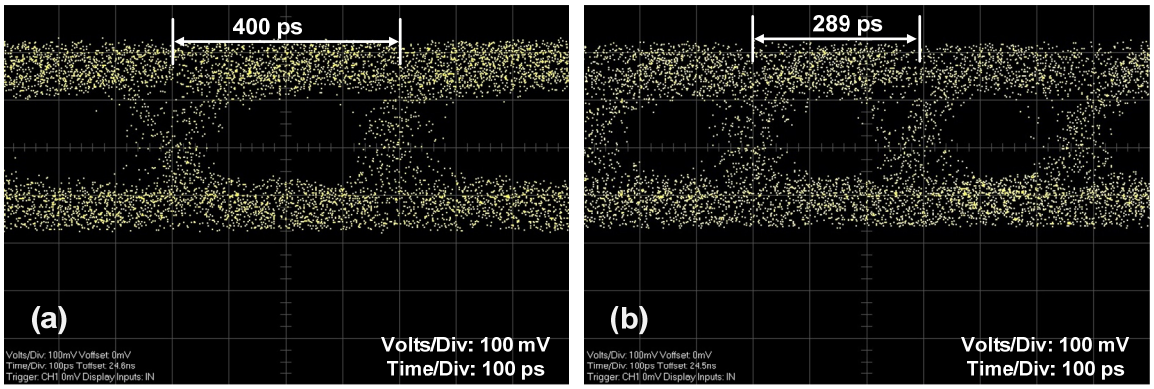

Figure 6.37: (a) Demodulated eye-diagram of the coherent demodulator at 2.5 Gbps; (b) Demodulated eye-diagram at 3.456 Gbps.

6.6 Summary

The performance summary of the multi-mode mixed-signal 60 GHz receiver is shown in Table 6.10. This design generation successfully demonstrates a 3.456 Gbps demodulation system using very-high-speed ADCs and DSPs in 90 nm CMOS technology. The maximum achievable speed is limited by the GBW associated with its technology. Nevertheless, this work demonstrates a digital processing power of less than 2 mW at multi-gigabit operation, which simplifies the overall system cost drastically.

Table 6.10: Performance summary of the multi-mode mixed-signal 60 GHz receiver.

Specification	Parameter		Unit
Supply voltage	1		V
RF front-end power	< 200		mW
IF front-end power	< 60		mW
I/Q ADCs	< 38		mW
DSP power	0.565 (ASK)	2 (BPSK)	mW
Maximum speed	1.728	3.5	Gbps
Maximum sampling rate	6.912		GS/s
Dynamic range	> 45		dB
Minimum sensitivity	-51	-56	dBm
RF locking range	5	30	MHz
Bit-error rate	1.5E-08 @ 864 Mbps 4.5E-08 @ 1.38 Gbps 9.0E-07 @ 1.728 Gbps	1E-12 @ 864 Mbps 1E-12 @ 2.5 Gbps 1E-12 @ 3.5 Gbps	—

CHAPTER 7

CONCLUSIONS

The final chapter lists the technical contributions of this research in developing high-speed low-power ADCs and mixed-signal demodulators using standard digital CMOS technology. Potential research directions for future related to this work are also presented.

7.1 Technical Contributions

The technical contributions of this research are as follows:

- The potentials of implementing a robust mixed-signal demodulator in CMOS technology are demonstrated. A design methodology to realize a high-speed RF/mixed-signal system is presented and verified from top-level specifications, system-level analysis, CMOS integrated circuits design, and eventually to on-wafer/module results. All phases of RFIC and ASIC design cycles are considered and studied carefully, leading to an unprecedented discovery.

- An ultra-low-power 3-bit ADC using two-channel, time-interleaved, flash architecture is implemented at 3 GS/s. The high-speed ADC, fabricated in digital 90 nm CMOS process, achieves a FOM of 0.35 pJ/conversion-step and 0.465 pJ/conversion-step at 3 GS/s and 5 GS/s, respectively. The measured power

consumption at 3 GS/s and 5 GS/s are 3 mW and 3.9 mW, respectively, leading to a potential use of multi-gigabit mixed-signal demodulator system, where low power consumption is the first priority.

- The demonstrated mixed-signal demodulator is a modification of the conventional hard-limited Costas loop architecture. By means of mixed-signal approach, scalability and power consumption are balanced compared to the all-analog or all-digital approach. The algorithm and complexity of a signal processing unit can be enhanced and expanded easily in digital domain. The use of XOR logic, as a phase discriminator, preserves the functionality of an analog multiplier at the same time maintaining low power budget. Its simplicity leads to small loop latency at high speed, which secures the stability for a closed-phase-recovery loop.

- The measured power consumption of the coherent DSP is only 2 mW at a nominal sampling rate of 2.97 GHz, indicating the most power-efficient DSP at multi-gigabit operation with a gate count of less than 200. Together, the measured power consumption, including the ADCs in I-path and Q-path, and a high-speed DSP, consumes a power consumption of 8 mW.

- The first fully-integrated mixed-signal demodulator, consisted of a 13 GHz QVCO, I/Q mixers, baseband VGAs with AGC and DC offset compensation loops, mixed-signal data converters, and a DSP, features a power budget of 60 mW and is capable of demodulating a multi-gigabit BPSK modulated signal up to 2.5 Gbps error-free transmission. This demonstrates for the first time a unique

multi-gigabit mixed-signal system that achieves fully on-chip digital synchronization without external processing and synchronization control. Real-time HD video streaming at 1.485 Gbps is also demonstrated.

- A high-performance fully-differential ADC is investigated and implemented at a sampling frequency of 6.912 GHz. The issue of the voltage offsets due to transistor random mismatch and PVT is alleviated by using resistive averaging network and DC correction circuit. The CMFB calibrates the output common-mode voltage of the T/H circuit to the middle level of resistor reference voltage, and forces the conversion process happening within the designed dynamic range. Low-*Vth* switch transistor and cross-coupled PMOS pair in parallel with diode load are chosen to improve overdrive recovery and to provide gain-boosting negative resistance as well as self-bias output common-mode voltage in the preamplifier and comparator stages.

- By oversampling the down-converted baseband signal at 6.912 GS/s constantly, a digital non-coherent ASK demodulation technique is implemented. The original binary data stream is recovered by simultaneously comparing the signal level in I/Q channels based on $I^2 + Q^2$ amplitude detection. Amplitude detection performs XNOR operation between the two MSBs in each channel and sums the results with an OR operator. This is equivalent of doing $I^2 + Q^2$ in analog domain. With merely an additional 565 μW to the overall power budget, the ASK demodulator achieves a BER of 1.5E-8, 4.5E-8, and 9E-07 at 864 Mbps, 1.38 Gbps, and 1.728 Gbps, respectively.

- A dual-mode, high-performance, mixed-signal demodulator is integrated with 60 GHz receiver front-end and fabricated in 90 nm CMOS technology. By incorporating the 6.912 GS/s ADC and employing two-channel time-interleaved topology throughput digital back-end, the coherent BPSK demodulator is able demodulate a BPSK modulated signal up to 3.5 Gbps error-free transmission with an improved minimum receiver sensitivity of -54.5 dBm. The proposed high-performance demodulator system is suitable for next-generation multi-gigabit transceivers using millimeter-wave frequency bands.

7.2 Conclusion and Future Work

The potential of broadband demodulator is immense as technology scaling pushes the overall power consumption of transceivers system even lower. The availability of the very-wideband spectra in millimeter-wave frequency bands, such as 60 GHz and 70-80 GHz, creates immediate opportunities for constant envelope single-carrier systems at multi-gigabit data rates. Hence, it is extremely critical that higher performance demodulator systems are developed to meet such requirements.

This research work has presented a mixed-signal 3.5 Gbps quadrature demodulator and finally integrated with 60 GHz receiver front-end for low-power millimeter-wave communication systems. The research conducted provides both system and circuit solutions to minimize the power consumption and complexity of receivers. At very-high speeds, it is found that a combination of system optimization and a hybrid

approach between analog and digital signal processing can lead to a very robust system. In additional, several design techniques are introduced to enable high-speed operation at very-low levels of current consumption. In the future, this research can be extended into the following areas: deeper examination of the digital algorithms and architectures used in transceivers, proper filtering to maximize SNR, and QVCO phase noise optimization to support higher-order modulation schemes.

A self-calibration digital algorithm is required to tune out transistor threshold mismatch due to deep sub-micron CMOS technologies (e.g., 32 nm), if higher resolution or smaller quantization level is desired. This directly affects the static and dynamic performance of ADCs. Without degrading the analog bandwidth in high-speed signal paths, calibration is best to be implemented at the reference voltages level. By varying the reference voltages in opposite direction to random offset voltages, offsets can be can be tuned out without bandwidth penalty. However, this approach requires overhead calculation time before normal ADC operation.

In the presence of additive stochastic noise, SNR can be maximized by implementing a matched filter in the baseband. This could lead to an improvement in minimum sensitivity and an increase in synchronization locking range of the current BPSK demodulator. Possible integration of higher-order anti-aliasing filters can be considered to replace the current first-order *RC* filter. However, at multi-gigabit data rates, the design of any filters could be a challenge.

The implemented quadrature down-converter is suitable to enable coherent QPSK demodulation based on the modified Costas loop architecture. This directly doubles the

data transmission speed without occupying more channel bandwidth. However, the quantization noise due to 3-bit resolution could be a limitation to enabling QPSK demodulation. Hence, a higher-bit resolution should be considered. In addition to quantization noise, oscillator phase noise could be a bottleneck to enable higher-order modulation schemes. Therefore, a lower noise QVCO is desired in the future.

Finally, to compensate the effects of atmospheric absorption and Friis's free-space propagation loss, this research work is only targeted for radio links in the millimeter-wave region using narrow-beam width and high-gain antennas in order to focus as much of the transmitted signal as possible onto the receiving antenna. When NLOS propagation is considered, the design and control of the beamforming phased array system are recommended. Two major challenges are likely to arise: the packaging and interconnect design to enable multiple antennas, LNAs, and PAs to coexist on a single substrate, and the control algorithms to control the directionality of the reception. The robustness of the multi-gigabit wireless transceiver can be greatly enhanced in a clustered environment.

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